SVT Sensors Inspection and Wafer Probing Test Plan

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I.A. Cali[1], A.Kostina[2], L.Tomasek[2]

Institution(s)

1 - Massachusetts Institute of Technology
2 - Czech Technical University

Abstract

The Inspection and Test Plan (ITP) covers wafer-level probing of the Monolithic Stitched Active pIXel (MOSAIX) and EIC-Large Area Sensors (LAS) prior to thinning and dicing. However, similar procedures can be applied also after this first thinning and dicing if required. The plan defines standardized test procedures and acceptance criteria to evaluate electrical functionality, verify design integrity, and detect process-related deviations at the wafer stage. The MOSAIX sensor is a wafer-scale monolithic pixel device developed in 65 nm CMOS technology with integrated analog front-end and digital readout circuitry across multiple stitched tiles. The EIC-LAS is a segmented derivative optimized for the ePIC Silicon Vertex Tracker (SVT) and designed for serial powering through an AncASIC, which provides local power regulation, bias generation, and control. Wafer probing will assess key parameters such as power consumption, bias currents, communication integrity, and pixel matrix functionality under nominal conditions, ensuring device quality, yield traceability, and readiness for subsequent thinning, dicing, and module integration.

Contents

List of Figures

1. SENSOR PROPERTIES

The **SVT (Silicon Vertex Tracker)** is developed as a well-integrated, large acceptance, high granularity, and low-mass tracking and vertexting system. The SVT consists of three regions with a total active area of approximately 8.5 m². The **Inner Barrel (IB**) and **Outer Barrel (OB)**, comprising three and two active layers respectively, cover the mid-central range, with their active volume extending radially up to about 42 cm. The active layers of the IB will be based on **MOSAIX (Monolithic Stitched Active pIXel)** sensors, while those of the OB will be equipped with **EIC- LAS (Large Area Sensor)** sensors. The SVT will also have 6 **Disks**, 3 per endcap, and they will be equipped with EIC-LAS.

The MOSAIX segment measures 265.992 x 19.564 mm. The MOSAIX top-level diagram is shown in Figure 1. The area comprises **LEC (Left-Endcap**), **REC** (**Right-Endcap**) and 12 **RSU** (**Repeated Sensor Units**). Each RSU is composed of 12 **Sectors (Tiles)**. The REC is a module with powering pads. LEC works as the main data collector and communication interface between the sensor and external systems. It includes 8 high-speed differential links, each with serializers that can transfer data at 10.24 Gb/s or 5.12 Gb/s. The LEC also provides power supply pads and differential I/O 2.56 Gbps links used for control. RSU includes the pixel arrays, bias, and readout logic.

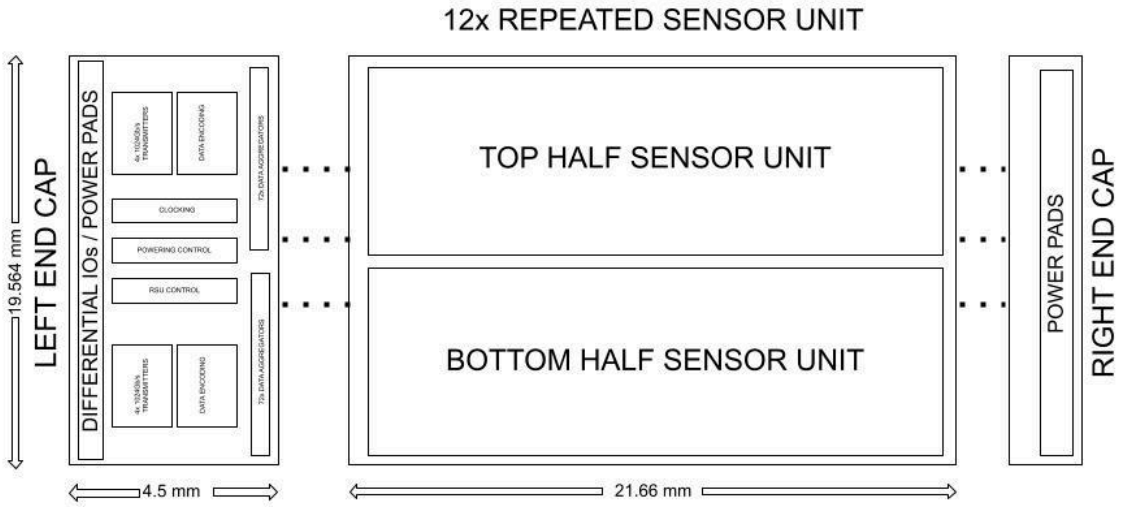

Figure 1. Top level diagram of MOSAIX

The MOSAIX was designed with the key specifications summarized in Table 2, which outline its main performance targets. Wafer quality control activities are required to validate device functionality and confirm compliance with the operational limits defined therein.

Property	**Specified / Typical Value**
Fill Factor	93% sensitive region
Pixel Performance	Detection Efficiency >99%; Fake hit rate <0.1 $pixel^{-1}$ s^{-1}
Data taking	4.4 MHz/cm^2 particle rate; 30.72 Gb/s off-chip data transmission; Minimum 2 μs integration time
Radiation Performance	10^{13} NIEL (1 MeV n_{eq}/cm^{-2}); 10 kGray TID; Triple Modular Redundancy
Power Budget (RSU)	40 mW/cm^2
Pixel Matrix Functionality	Pixel pitch ≈ 22.8 × 20.8 μm; 144 tiles (independent units)
Power Integrity / Domain Isolation	Multiple isolated domains
Data Serialization / Readout Speed	Configurable 5.12 or 10.24 Gb/s

Table 1. Sensor specifications

The MOSAIX chip uses four independent global power supplies and a reverse substrate bias. Three supplies and the substrate bias are distributed across the chip from both endcaps, while the fourth supply is dedicated to the LEC. List of power domains is in Table 2:

	Name	Description	Voltage (min, nom, max) [V]	Current at nominal [mA]	LEC/REC pads
Global	GDVDD	Global digital supply	1.17, 1.30, 1.37	1430	Yes/Yes
	GDVSS	Global digital ground			
	GAVDD	Global analog supply	1.17, 1.30, 1.37	540	Yes/Yes
	GAVSS	Global analog ground			
	GSVDD	Global services supply	1.19, 1.32, 1.39	227	Yes/Yes
	GSVSS	Global services ground			
	PSUB	Global substrate bias	-2, -1.20, 0		Yes/Yes
LEC	TXVDD	Serializer power supply	1.62, 1.80, 1.90	454	Yes/No
	TXVSS	Serializer power ground			

Table 2. Power domains of MOSAIX

The EIC-LAS will have the same design specs of MOSAIX and the same architecture of LEC, RSUs and REC. The EIC-LAS will be designed in 2 flavors, 1 with 5 RSUs and 1 with 6 RSUs.

The MOSAIX and EIC-LAS sensors are advanced CMOS (Complementary Metal Oxide Semiconductor) devices developed for the ALICE ITS3 (Inner Tracing System 3) detector and ePIC Silicon Vertex Tracker (SVT) and require precise wafer-level testing to ensure full electrical functionality before mechanical processing. The testing procedures and wafer probing equipment for MOSAIX and EIC-LAS will be identical, as both share the same functionality and interfaces; the only difference in interface is that EIC-LAS features a reduced number of data links but it is expected to have the same pinout.

The MOSAIX and EIC-LAS device performance must be evaluated across multiple functional domains. In particular, attention will be given to the powering of the LEC and Tile sections, the LEC response in terms of communication and control register operation, and the Tile response in terms of both electrical and sensor performance.

This document describes the characterization procedures for individual MOSAIX and EIC-LAS devices. Three initial performance categories will be defined:

- **Gold**;
- **Silver**;
- **Bronze**.

To classify devices according to measured functionality and response. A score will be given to each characterization step and the global performance will be evaluated considering the lower score of the list. The scores of each step will be recorded and associated with each classification.

It is anticipated that, during the testing phase, additional categories may be introduced to allow finer performance granularity if required. The full list of acceptance criteria, and their quantitative definition will be based on results from the MOSAIX pre-production series wafer probing, ahead of **Quality Control (QC**) for production wafers.

A final classification will be assigned to each sensor assembly based on the performance of its constituent sensor units (see section 3 for more details). The QC procedure described in this document will guide sensor selection for detector integration.

2. Processes and Procedures MOSAIX/EIC-LAS sensors

The qualification of MOSAIX / EIC-LAS sensors involves a comprehensive sequence of electrical, functional, and performance tests conducted during wafer probing and subsequent assembly steps after thinning and dicing. These include power domain verification, slow-control communication checks, reset and configuration validation, pixel matrix functionality tests, data readout and optical link characterization, as well as final device grading. This structured testing flow ensures that each device meets design specifications, maintains operational reliability, and is properly classified for integration into the SVT.

2.1. Visual inspection

Visual inspection is performed on all MOSAIX and EIC-LAS wafers immediately after delivery and intended as check-in phase and prior to electrical wafer probing. The inspection identifies mechanical or surface defects that may affect probe contact reliability, electrical measurements, or subsequent processing steps. During the inspection, the following features are systematically evaluated:

- **Wafer planarity:** any deviation exceeding **40 µm** from nominal flatness is considered **non-conforming**. Such wafers may not be compatible with the probe station; an investigation must be conducted to determine whether local re-clamping or alternative probing strategies are feasible.

- **Surface condition:** scratches, delamination, chipping, or residue on the wafer surface are assessed on a **case-by-case** basis, with priority given to **rejecting wafers** that exhibit damage across functional areas.

- **Particle contamination:** any visible foreign material, residues, or processing debris are noted and, where possible, removed under clean conditions before probing.

- **Probe pads:** pad size, alignment, and metallization quality must conform to design specifications. Damaged or contaminated pads, incomplete passivation removal, or edge defects around the passivation opening are grounds for rejection.

- **Sensor edges:** verify proper cleaning and passivation removal around die edges; poor edge preparation can cause contact instability or debris release during probing.

2.1.1. In-Process Testing

The visual inspection is performed as an in-process test at the beginning or prior to the wafer probing phase. Each wafer is examined prior to probing to verify its condition and suitability for testing. This procedure confirms mechanical integrity and surface quality, ensuring the wafer and sensors meet the required standards, before any electrical bias or measurements are applied. The inspection can be carried out using different methods depending on equipment availability — either through an automatic topography scan on the probe station (built in microscope with magnification > x 5) as a built-in feature or by cross-checking with an external 3D optical microscope with magnification of x5 to assess wafer planarity, surface defects, and pad geometry in greater detail.

2.1.2. Verification Testing and classification

Following in-process inspection, selected wafers may undergo **verification re-inspection** after probe testing to confirm that no damage occurred during contact operations. This visual verification validates handling procedures and the mechanical robustness of the wafer surface and metallization layers. Following visual inspection, wafers are categorized into three qualification classes based on the proportion of functional sensors and overall physical condition:

- **Golden** — Wafers where **five** MOSAIX or **≥ 90%** of EIC-LAS meet quality and structural integrity requirements. This includes the absence of wafer-edge chipping, passivation layer residues, surface scratches, or other defects that could impact probing or electrical performance. Golden wafers are released for electrical testing.
- **Silver** — Wafers where **four** MOSAIX or **≥ 50% but < 90%** of EIC- LAS are deemed functional and probe-ready. These wafers typically exhibit localized contamination, minor surface damage, or partial passivation residues. They may require limited rework (e.g., cleaning or localized surface treatment) followed by re-inspection prior to testing.
- **Bronze** — Wafers where **three or less** MOSAIX or **< 50%** of EIC-LAS comply with the qualification criteria. Significant mechanical damage, widespread contamination, or structural defects render these wafers unsuitable for standard probing. Bronze wafers are excluded from the production flow and may be repurposed as dummy wafers for equipment calibration, process tuning, or training purposes.

2.1.3. Failures and Non-Conformances

If a wafer exhibits cracks, delamination, missing pads, significant contamination, or any other condition that prevents reliable probing, it is classified as **non-conforming**. The wafer ID, defect description, and classification category are recorded in the inspection log, and the wafer is

immediately segregated from the production flow. Minor issues such as removable contamination may be addressed through rework and subsequent re-inspection. Wafers classified as **Bronze** - typically exhibiting severe mechanical damage or with less than 50% functional dies - are considered damaged and unsuitable for standard testing. Such wafers are rejected from testing and may be repurposed as dummy wafers for equipment setup, calibration, or process validation. All corrective and follow-up actions are documented in accordance with the quality control protocol.

2.2. Powering testing

The Powering Test verifies the overall electrical integrity, stability, and communication functionality of the device before full functional evaluation. It combines sensor characterization, power consumption validation, epitaxial-layer integrity checks, and digital configuration verification to ensure that all power domains operate within specification and that communication interfaces respond as expected. Before any advanced performance characterization, these tests are executed at the wafer level. The sensors operate with four independent global power supplies and a reverse substrate bias. Three of these supplies, along with the substrate bias, are distributed across the entire chip and delivered from both endcaps, while the fourth supply is localized exclusively within the LEC (see table 2).

Successful power-up requires a **defined power-up and reset sequence** to ensure that the analog front-end, digital core, slow-control buses, serializers, tiles, and auxiliary services initialize in a known state and correct order. The procedure begins with powering and releasing the Service domain from reset — including the GSVDD supply, global clock distribution, and the Services Slow Control (SSC) interface. Once the service infrastructure is stable, high-speed channel clocks and serializers are enabled, and Substrate Bias Buffers (SBB) are initialized. Finally, each tile's local power domains are activated and their per-tile resets are de-asserted.

2.2.1. In-Process Testing

To validate power domain stability and functional integrity across key operating points, dedicated powering tests are performed for each global supply — **GSVDD**, **GDVDD**, **GAVDD**, and **TXVDD** — using both **step-ramp** and **no-step ramp** procedures. At each voltage point, the procedure involves:

- Applying the supply voltage directly to the target level.
- Monitoring and recording **inrush current**, **steady-state current**, and any abnormal transient behavior.
- Powering down the device and logging all measurement results for analysis.

This methodology ensures consistent characterization of each supply domain under controlled conditions and verifies correct device behavior across the full operational voltage range.

2.2.2. Verification and Classification

Based on these measurements and functional checks (including service domain activity, serializer lock, and communication readiness), devices are categorized into three qualification classes:

- **Golden**, when all parameters are within specification and the sensor exhibits nominal behavior;

- **Silver**, when minor deviations are observed but operation remains stable after rework or reset;
- **Bronze**, when critical parameters fall outside acceptable limits or functionality cannot be restored. Bronze devices are excluded from use and may be repurposed as dummy components for equipment setup or process calibration and debugging.

Acceptance Criteria:

- Steady current within **±15 %** of nominal.
- Inrush ≤ 1.5× steady-state for < 1 ms.

Table 2. presents the expected current consumption breakdown for each MOSAIX supply net. For the analog (**GAVDD**) and digital (**GAVSS**) domains. A similar table will be provided for EIC-LAS once available.

2.2.3. Failures and Non-Conformances

A sensor or wafer is considered **non-conforming** if any of the following occur:

- Power does not assert within the expected voltage or time window.
- Excessive current or inrush beyond limits.

Non-conforming wafers are logged in the inspection record and excluded from further probing. Affected samples may be re-tested once after setup verification; persistent failures are flagged for process review and possible return to fabrication for analysis.

2.3. Slow Control SRV and Electrical Integrity

The **Slow Control Service (SRV) tests** verify correct operation of the on-chip control and configuration interface when the SRV domain is powered, while global system domains remain off. These tests ensure that the SRV remains responsive, can correctly read and write configuration registers, and maintains communication stability across the full **GSVDD range of 1.08 V, 1.20 V, and 1.32 V**. Testing at these voltages with **SRV ON and GLOBAL OFF** isolates the slow control functionality to confirm robustness under partial power conditions. Electrical integrity tests assess signal integrity, timing margin, and power domain robustness when multiple SRV endpoints (EPs) are active simultaneously. Testing is conducted at wafer level to identify early electrical instabilities.

2.3.1. In-Process Testing

The SRV tests are conducted during wafer probing following the verification of the GSVDD domain. For each voltage setpoint (**1.08 V**, **1.20 V**, and **1.32 V**), only the SRV power is enabled while all other global domains remain disabled. Communication with the device under test is established via the slow control interface, with data readout and command execution handled through the **Enclustra Arria 1–based control board**. The SRV is then exercised using a predefined command sequence to verify proper power-up behavior, communication responsiveness, and read/write register access.

Electrical integrity tests are performed after verification of SRV and LEC functionality. The SRV stress sequence is executed through Enclustra Arria 1–based control board while monitoring supply current,

communication status, and error counters. The tests are conducted at nominal, minimum and maximum supply levels to capture any voltage-sensitive failures. Clock gating patterns are used to simulate dynamic power domain switching and verify that no data corruption or communication drop occurs during clock transitions.

2.3.2. Verification Testing

A **custom-developed software framework** will be used to perform a series of functional tests, executing an automated sequence of procedures that can also be run individually when required. Tests are performed at each voltage level to validate different aspects of SRV performance:

- **SC SRV Alive Test** – Confirms that the SRV domain powers up correctly and responds to a ping or status command.
- **SC SRV Read/Write Test** – Verifies correct operation of configuration registers by writing known patterns and reading them back without data corruption.
- **SC SRV Gate Test** – Tests command gating and access control to ensure proper enable/disable behavior under isolated SRV conditions.
- **SC SRV Broadcast Test** – Validates broadcast functionality by sending a command to multiple addressable blocks and confirming uniform response.
- **SC SRV Stress Test** – Runs extended sequences of back-to-back commands to evaluate timing margins and communication reliability over time.

Three configurations are evaluated to cover all key SRV endpoints:

- **SC SRV Stress Test with Clock Gating – LEC SRV EP**
  Confirms that the LEC SRV endpoint remains functional during repeated clock enable/disable cycles.
- **SC SRV Stress Test with Clock Gating – LEC ADC EP**
  Evaluates ADC endpoint stability, verifying data path retention and recovery after gated clock intervals.
- **SC SRV Stress Test with Clock Gating – SRV NODE EP ×48**
  Runs high-load parallel stress on all 48 SRV node endpoints, measuring response latency, communication throughput, and current variation under switching activity.

Acceptance Criteria:

- Continuous SRV responsiveness during and after clock transitions and remains fully functional at all three voltage levels.
- No CRC, parity, or timeout errors during stress sequences.
- Supply current variation $\leq \pm 10$ % between active and gated states.
- All endpoints recover nominal operation within **< 100 ms** after clock re-enable.

2.3.3. Failures and Non-Conformances

During slow control validation, each die is tested for reliable communication, configuration integrity, and command execution. Failures in this stage may include **loss of SRV communication**, **incorrect register readback**, **gate response errors**, or **broadcast inconsistencies**. If such an event occurs, the

test sequence is repeated once after verifying probe contact quality, supply stability, and signal integrity. Devices that continue to fail after re-testing are classified according to their severity:

- **Golden** sensors demonstrate stable slow control operation with correct readback and consistent broadcast behavior;
- **Silver** sensors may exhibit minor recoverable issues (e.g., requiring re-initialization or a repeated command sequence) but function correctly after corrective action;
- **Bronze** sensors show persistent communication loss, unresponsive gates, or unrecoverable protocol errors and are excluded from further functional testing, but still can be used as dummy sensors for debugging.

All failure events must be documented with the voltage level, and failure type for traceability, process review, and root-cause analysis.

2.4. LEC Functionality

The LEC Functionality tests verify that all subsystems within the LEC - including **MGTM (Management/Timing)**, **SRV**, **NODE**, **EP SerDes (End-Point Serializer/Deserializer)**, and **ADC blocks** - respond correctly to reset commands and return to defined default states. This ensures proper synchronization and reliable startup behavior of the system before full functional operation. Testing focuses on validating the internal reset propagation, register integrity, and SerDes reinitialization.

2.4.1. In-Process Testing

The reset functionality tests are executed during wafer probing following the verification of power delivery and slow-control operation. Each LEC sub-block is subjected to a controlled reset sequence via the **SRV interface**, with register write and readback operations performed through the **Enclustra Arria 1–based board**. All electrical signals generated during this process are propagated to the **FMC connector**, enabling reliable communication, monitoring, and control. Throughout the test, status flags, register contents, and serial link readiness are continuously monitored to confirm that all LEC blocks initialize deterministically from a known state after power-up

2.4.2. Verification Testing and Classification

The following tests are performed at nominal operating conditions to validate LEC reset and control logic:

- **Reset MGTM Test** – Issues a master reset to the MGTM (Management/Timing) block and verifies successful recovery of clock and synchronization status.
- **Reset LEC SRV Register File** – Resets all SRV configuration registers within the LEC domain and confirms default register values.
- **Reset SRV NODE EP SerDes** – Validates proper reinitialization of the SRV node and endpoint serializer/deserializer following a soft or hard reset command.
- **Reset LEC ADC EP SerDes and Register File** – Performs a full reset of the ADC endpoint, associated SerDes, and configuration registers, ensuring data paths return to their nominal idle state without lock-up or corruption.

- **Data Link performance test -** This test evaluates the integrity, stability, and overall performance of the high-speed optical interfaces. All eight links are tested across the full range of supported data rates — 5.12 Gbps, and 10.24 Gbps — as well as all operational intermediate combinations to ensure reliable functionality under all configuration scenarios, PRBS, etc.

Acceptance Criteria:

- Each sub-block responds to reset within **< 100 ms**.
- All configuration registers return to **default values**.
- Serializer/Deserializer links re-lock successfully after reset.
- No unexpected current draw or error flags after reset completion.
- Eye diagram analysis must demonstrate a clear, open eye with acceptable timing margins and jitter

Depending on the results of the reset validation and optical link performance tests, devices are categorized into three qualification classes:

- **Golden** devices meet all acceptance criteria, including reset response, register integrity, stable SerDes re-lock, nominal current behavior, and a fully open eye diagram within specification.
- **Silver** devices show minor recoverable deviations — such as slightly extended reset time, reduced eye margin, or marginal BER — but achieve compliant performance after next try.
- **Bronze** devices fail to meet one or more critical criteria, such as persistent communication errors, closed eye diagrams, or excessive BER, and are excluded from production use, though they may be repurposed as dummy components for debug or setup activities.

2.4.3. Failures and Non-Conformances

Failures may include missing reset acknowledgment, incorrect register values after reset, link instability, or persistent fault indicators. In the event of such issues, the test is repeated once after verifying power integrity, communication interfaces, and test setup conditions. Devices that continue to exhibit malfunction after re-testing are classified as **Bronze**, indicating non-conformance with the acceptance criteria. These dies are excluded from the qualified lot and may be repurposed for debug, calibration, or setup activities.

2.5. Pixel Matrix test

Pixel matrix tests are designed to validate the functionality, signal integrity, and data transmission performance of the front-end pixel array. These procedures examine the system's ability to read data, manage pixel masking and unmasking, respond to controlled digital pulses, and maintain correct operation under various clocking and gating scenarios. Additionally, parallel data readout tests ensure that large-scale acquisition and backend data handling meet performance and reliability requirements. Together, these tests provide comprehensive coverage of the pixel matrix's digital logic, communication interfaces, and robustness against functional and electrical faults. The final detector design aims for a high fill factor, representing the fraction of area covered by active pixels. The powering yield is defined by requiring that **less than 2%** of the sensitive area can be powered down due to local defects.

2.5.1 In-Process Testing

During wafer probing, a series of in-process tests are carried out to verify the fundamental functionality and readiness of the pixel matrix before full qualification. These tests check data packet generation and backend reception, validate masking and unmasking behavior, and assess the matrix response to digital pulses. They also evaluate electrical integrity under different clock conditions and verify proper functionality with clock gating enabled. Together, these checks provide an early assessment of pixel performance and help identify potential issues before comprehensive verification. It should be noted that localized regions of dead pixels can obstruct data flow and potentially block the readout, highlighting the importance of early detection during in-process testing.

2.5.2. Verification Testing and Classification

During evaluation, the following tests have to be performed under nominal operating conditions to assess pixel-level functionality :

- **Pixel Matrix Read Test:** Generates packets from the pixel matrix and verifies correct reception on the backend, while checking for noise or spurious signals.

- **Pixel Matrix Mask / Unmask Tests:** Validates masking logic. In the **Mask Test**, pixels are masked and should remain inactive. In the **Unmask Test**, pixels are unmasked without pulsing to ensure no unintended activity occurs.

- **Pixel Matrix Digital Pulse Test:** Stimulates the matrix using a checkerboard pulse pattern with the DAC tuned to the maximum threshold. Data packets are read out and analyzed for integrity and **SEU (Single Event Upset)** counter behavior.

- **Pixel Digital Pulse Tests (40 MHz / 20 MHz):** Evaluates electrical integrity under different clock frequencies. SEU counters should remain stable with no increments if the system functions correctly.

- **Pixel Matrix Digital Pulse Test with Clock Gating:** Repeats digital pulse testing with clock gating enabled on domains **A**, **B**, and **C**. Functional variations are analyzed. This is a non-blocking test but contributes to yield statistics.

The number and distribution of bad pixels must be recorded, as they can impact readout performance and overall detector functionality.

Results from these tests are used to verify device functionality and categorize pixel matrix performance:

- **Gold:** The sensor demonstrates **full functionality** with **less than 2% of its sensitive area powered down** due to local defects. No unexpected noise is present, masking and unmasking behave as intended, and SEU counters remain stable (except in clock-gated conditions where increments are expected).

- **Silver:** Up to **2% of the sensitive area** may be powered down or show recoverable defects. Minor issues such as transient SEU counter increments or slight timing deviations may occur but are

resolved after reconfiguration, reset, or recalibration.

- **Bronze:** More than **2% of the sensitive area** is powered down or shows persistent malfunction. Critical failures such as continuous noise, SEU counter increments during normal conditions, or loss of masking logic are observed. These dies are excluded from detector integration but may be repurposed for debugging or setup validation.

2.5.3. Failures and Non-Conformances

Failures may include packet errors, data corruption, masking faults, unexpected SEU increments, etc. The test is repeated once after confirming probe contact, power, and configuration. Devices with persistent errors are classified as **Bronze** and marked as non-conforming.

3. Final Device Grading and Sensor Assembly Classification

Following individual wafer-level testing and qualification, each MOSAIX/EIC-LAS device is assigned a final quality classification — **Golden**, **Silver**, or **Bronze** — based on its measured performance across power domain behavior, slow-control operation, pixel matrix functionality, and data readout integrity. This classification is recorded in the database and used as the basis for subsequent sensor assembly decisions.

The IB layers, L0/L1/L2, will be equipped with sensors made of 3/4/5 MOSAIX segments, respectively, diced together from the same wafer. The overall classification of these sensors is to be determined by the quality grades of the individual segments according to the following criteria:

- **Golden Sensor:** All integrated devices are classified as **Golden**, meeting all functional, electrical, and performance requirements. These sensors are fully qualified for installation in the detector.

- **Silver Sensor:** At least one integrated device is classified as **Silver**, exhibiting minor deviations that remain within acceptable operational margins. Such sensors are suitable for integration but may require additional calibration, tuning, or software compensation during operation.

- **Non-Qualified Sensor (Bronze):** The presence of any **Bronze** device — indicating non-conformance or significant performance degradation — disqualifies the sensor from deployment in the final detector. Assemblies containing Bronze devices, however, may still be repurposed for **debugging, validation, or software development** purposes.

This classification framework ensures consistent traceability from individual segment characterization to complete sensor integration, supporting quality assurance, performance optimization, and reliable detector construction.

4. Experimental/Test Setups

The wafer-level tests for the MOSAIX and EIC-LAS sensors are conducted using precision probe stations and controlled laboratory instrumentation to ensure measurement repeatability and compliance with electrical test standards. The same general experimental setup is employed for all test types described in this plan, including powering, communication, and functionality verification.

4.1. Experimental Method Overview

All measurements are performed on a semiautomated probe station equipped with a high-resolution optical microscope, motorized chuck, and multi-camera alignment system. The specific model may vary depending on laboratory availability (e.g., MPI TS-series or FormFactor CM300xi). The wafer is securely mounted on the vacuum chuck, aligned using optical fiducials, and contacted through a **dedicated probe card** designed for the MOSAIX and EIC-LAS pad layouts.

A custom-developed, web-based software platform will be used to manage and execute all wafer-level tests and subsequent QC tests after thinning and dicing. The system will provide a shared testing framework for all device types, ensuring consistency across testing procedures while remaining modular and expandable for future production needs. Dedicated control and test modules will be implemented for each functional block of software, allowing both automated and manual test execution. The platform will also include integrated analysis tools to evaluate performance metrics and verify compliance at every testing stage.

In addition to test control, the software will serve as a management system, interfacing with an underlying SQL database to store and retrieve key information such as entities, test configurations, measurement data, and results. At the time of writing a SVT private version database hosted at CERN is used but it is expected to be migrated to a global ePIC construction database once available.

Power, control, and measurement signals are routed through precision cables and shielded connections to minimize electrical noise and ensure stable biasing. The test control software coordinates wafer stepping, bias application, data logging, and result storage for traceability and automation.

The testing will be performed using the setup illustrated in Figure 2, in combination with the custom-developed software. A simplified diagram of the system typically includes a probe station equipped with a dedicated probe card, source measurement units (SMUs) and programmable power supplies for biasing, as well as an oscilloscope, Enclustra Arria 1 based board and a control PC running automated software that manages the overall test sequence and data acquisition.

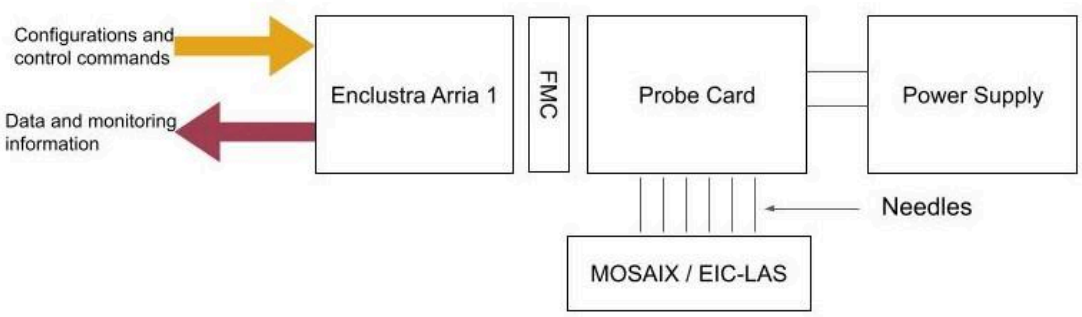

Figure 2. Block diagram of the Setup

A prototype of the system has already been developed using the NKF7 serializer and its dedicated vertical probe card, with the clock provided by an external generator and the output signals read out directly by an Enclustra module via SMA inputs. On the Figure 2 below that shows the vertical probe card, featuring dedicated connectors for power connections, differential outputs, clock input, and configuration jumpers.

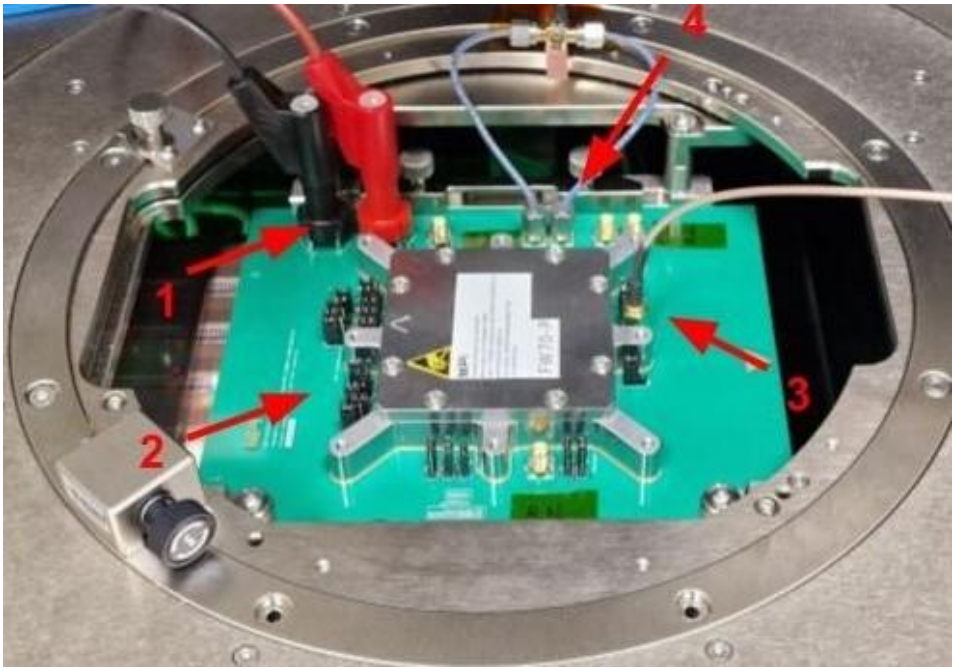

Figure 3. Serializer (NKF7) vertical probe card, where 1 - power connectors, 2 - configuration jumpers, 3 - Clock, 4 - differential output

The technology required to achieve 10.24 Gb/s wafer probing has been validated with the NKF7 serializer. As shown in the oscilloscope measurement (12 GHz, differential probe) on Figure 3, the signal

quality remains robust and stable, even after multiple contact iterations, demonstrating the reliability of the high-speed readout interface. With the current test setup, it is not possible to perform PRBS measurements. However, the adherence of the results obtained with the one expected from simulation and specs of the boards hints that system architecture provides reliable means for precise electrical characterization and high-speed data validation of the MOSAIX and EIC-LAS devices.

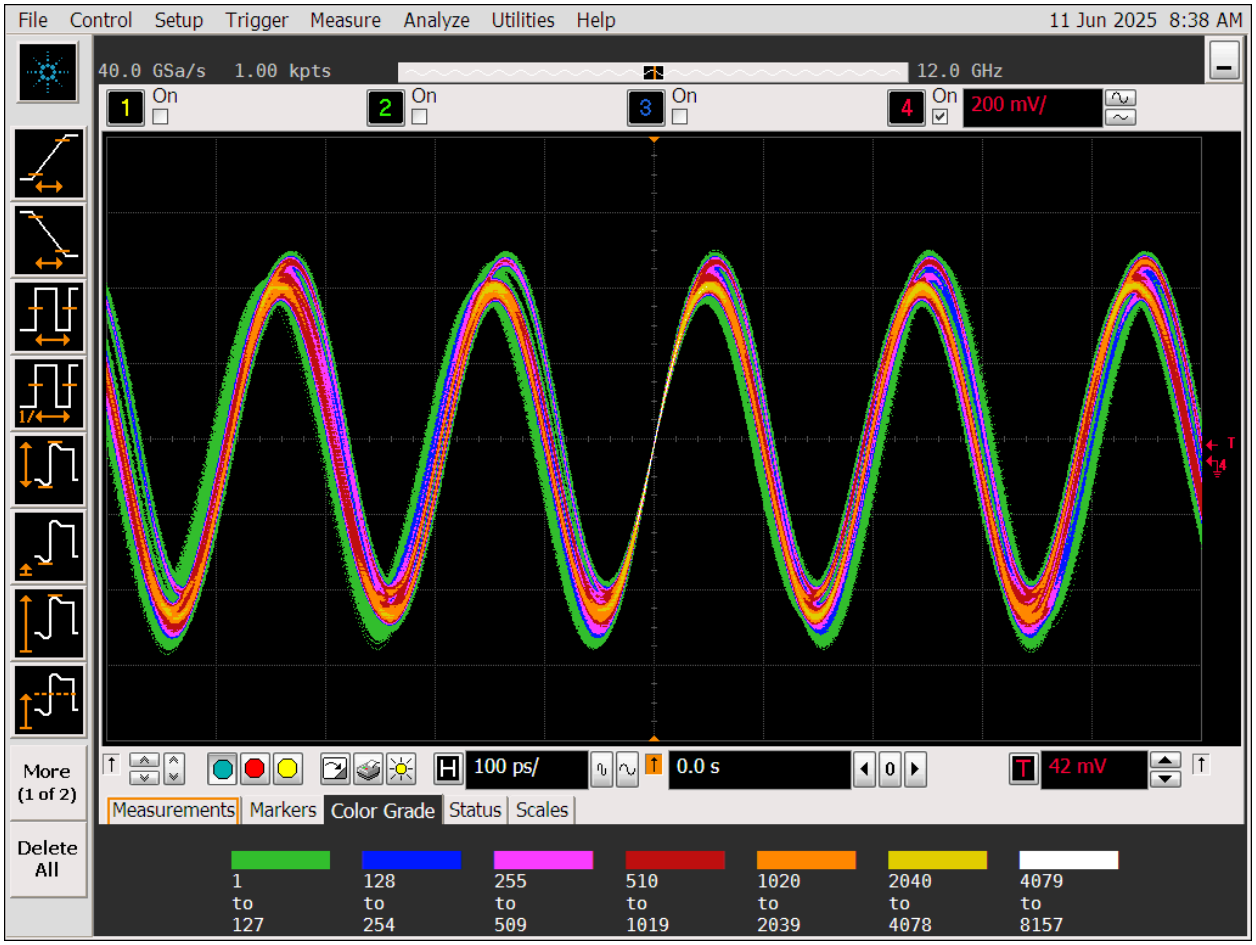

Figure 4. Signal output from Agilent oscilloscope

4.2. Resource Requirements

The following infrastructure resources are required to safely operate the wafer-level test setup:

- **Clean, ESD-controlled work area** (Class 1000 or better recommended)
- **Stable AC power** suitable for the instrumentation and probe station, depending on regional laboratory standards.
- **Compressed air and vacuum supply** for chuck operation and wafer handling
- **Temperature-controlled lab environment** (typically 22 ± 2 °C)
- **Proper grounding and static discharge protection** for all electrical equipment

4.3. Test Conditions

Testing is performed under controlled laboratory conditions to maintain measurement accuracy and device reliability:

- **Humidity:** < 50 % RH, ESD-safe conditions
- **Lighting:** Diffuse optical illumination for visual inspection
- **Vibration:** Minimal mechanical vibration (< 1 μm) to maintain probe stability
- **Wafer Handling:** All wafers handled with a vacuum wand and stored in clean carriers

All tests will be performed at room temperature (22 ± 2 °C), as the sensors have been shown to demonstrate optimal and stable performance around 25 °C.

4.4. Equipment

All specialized equipment necessary to carry out the tests described in Table 3. All equipment must be calibrated and certified according to institutional standards before use. Where applicable, safety checks and interlocks must be verified before test execution.

Equipment	Function / Description / Specification	Model / Example
Probe Station	Wafer probing platform with optical microscope and capability for vertical probing	MPI TS 3500 SE / FormFactor CM300xi
Probe Card	Interfaces wafer pads to test instruments; includes vertical spring-loaded needles	Custom-designed for MOSAIX / EIC-LAS
Source Measure Units (SMUs)	Precision voltage/current sourcing and measurement for domain-level testsıo Resolution ≤100 fA,	Keysight B2900 / Keithley 2600 Series
Programmable Power Supplies	Provides stable, low-noise DC bias to analog, digital, and service domains. Ripple <1 mV rms, resolution 1 mV / 1 mA, accuracy ±(0.01% + 1 mV).	Keysight N6700B / HAMEG HMP4040
Test Control Computer	Automates probing, bias sequencing, and data logging	Linux with USB connections

ESD Protection Equipment	Ensures operator and equipment safety during testing	Wrist straps, mats, ionizer

Table 3. Equipment specifications

After each testing phase wafers are stored and handled under controlled cleanroom conditions to maintain mechanical integrity and prevent contamination.

For short- and medium-term storage, wafers are placed in Front Opening Shipping Boxes (FOSBs), which are standard containers used across semiconductor facilities for the safe storage, transport, and handling of wafers and similar substrates (e.g., sapphire or other single-crystal materials).
Each FOSB can accommodate up to 25 wafers and provides ESD protection, particle control, and mechanical isolation during transfer between testing stages.

All containers are clearly labeled with wafer ID, processing stage (pre-/post-thinning), and QC classification, ensuring full traceability throughout the experimental workflow.

5. Environment, Safety & Health Considerations

All procedures described in this document are carried out in accordance with the **Environment, Safety, and Health (ES&H)** policies of the relevant laboratories and work areas. Activities are implemented following the established **Work Planning and Control** frameworks of the participating institutions:

- At **Brookhaven National Laboratory (BNL):** Activities are conducted under the *Standards-Based Management System (SBMS)* — "Work Planning & Control for Experiments and Operations."

- At **CERN:** Procedures follow the *CERN Safety Rules* and the *Safety Policy Framework* (*Safety Code F* and associated Safety Instructions), which govern laboratory operations, equipment use, and personnel protection.

- At **Czech Technical University (CTU):** Activities comply with the university's *Occupational Health and Safety Management System*, ensuring adherence to national regulations for laboratory safety and radiation protection.

- At **Brunel University London:** Experimental work is performed under the *Health, Safety and Environment (HSE) Management System*, which defines institutional requirements for risk assessment, safe laboratory practice, and personnel protection.

- At **Oak Ridge National Laboratory (ORNL):** Work is carried out according to the *Integrated Safety Management System (ISMS)*, ensuring compliance with U.S. Department of Energy (DOE) regulations and the safe execution of experimental activities.

All work is performed by trained personnel using approved equipment and best laboratory practices to minimize risk to both individuals and materials. Work areas are kept clean, organized, and ESD-controlled to prevent contamination or mechanical damage to wafers and test hardware.

The following **personal protective equipment (PPE)** and materials are mandatory during all wafer handling and electrical test operations:

- **Powder-free nitrile gloves** – to prevent contamination and protect devices from electrostatic discharge (ESD).
- **Safety glasses** – to protect against accidental contact with optical instruments or debris.
- **ESD shoes** – to prevent electrostatic discharge during wafer handling and probing operations

All activities described herein must comply with institutional safety policies and be carried out under approved work permits or task authorizations, where applicable. Regular reviews of laboratory conditions and equipment safety must be conducted to ensure ongoing compliance and to maintain a safe working environment for all staff and collaborators. The entire test environment is shielded against light and radiation to ensure safe operation and reliable measurements when radioactive sources are used.

6. Records and Documentation

All inspection and test activities for the MOSAIX / EIC-LAS wafer-level program — including powering tests, slow control verification, visual inspection, pixel matrix evaluation, power-on reset checks and functional performance assessments — will be fully documented in accordance with internal project requirements and partner laboratory quality systems. A dedicated custom-developed software tool will coordinate the execution of these tests, retrieve parameters from a centralized database, and store all results back into it, ensuring full traceability and repeatability. Following the completion of the testing campaign, the wafer yield will be evaluated, a comprehensive functional wafer map will be produced, and the sensors will be classified according to their measured performance parameters.

For each manufactured wafer lot or device batch, the foundry or supplier is responsible for maintaining fabrication travelers and process logs that describe:

- Raw materials and lot numbers used during wafer fabrication.
- Process parameters, recipe versions, and inspection checkpoints.
- Results of in-process electrical, mechanical, or optical inspections.
- Wafer acceptance data and summary yield reports.

Temporary or intermediate documents such as setup notes, temporary measurement screenshots, or internal data scratch files do not need to be archived permanently unless they directly support a specific test anomaly or non-conformance. Relevant transient documents linked to a test event must be referenced in the final test report and attached to the corresponding wafer lot record. Any updates, deviations, or revisions to these procedures must be version-controlled and logged in the group documentation archive (e.g., Git, SharePoint, Dropbox).

All results from the performed tests are recorded for traceability. Following these test phases, wafers are stored under controlled environmental conditions to preserve integrity. Subsequent handling, distribution, and shipping activities fall outside the scope of this document.

7. References

Collaboration ALICE. Technical Design report for the ALICE Inner Tracking System 3 - ITS3 ; A bent wafer-scale monolithic pixel detector. Technical report, CERN, Geneva, 2024.

8. Glossary

SVT - Silicon Vertex Tracker
MOSAIX - Monolithic Stitched Active pIXel
LAS - Large Area Sensor
ITS3 - Inner Tracing System 3
LEC - Left Endcap
REC - Right Endcap
RSU - Repeated Sensor Units
QC - Quality control
IB - Inner Barrel
OB - Outer barrel
SBB - Substrate Bias Buffers
SRV - Service
MGTM - Management/Timing
EP - End-point
SerDes -Serializer/Deserializer
SC - Slow Control
PPE - Personal protective equipment
ESD - Electrostatic Discharge
FOSB - Front opening shipment box