TOF Stavelet/Module Inspection and Test Plan

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Abstract

Stavelets for the time-of-flight barrel detectors are assembled as modules in multiple sites. The QA/QC will be done first on components (electrical, visual), then after assembly (metrology) and finally on the completed stavelet (ASIC charge collection). Stavelet are shipped to stave assembly site where they are loaded on the half stave, then QA/QC is performed. Finally, two half staves are joined on the backside to fabricate the final double-sided stave.

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1. STAVELET PROPERTIES

The module of the BTOF is referred to as ‘stavelet’, it is made from an interposer board loaded by sensor, ASIC (FCFD) and minimal electronic components. The assembled stavelets will be loaded on a stave on both sides of the stave, each side will have 7 stavelets and a Service Hybrid loaded. The cooling is provided by a pipe running inside the stave. Figure 1 shows the exploded view of a stave. The fully loaded stave total thickness will be around 7-8mm with a material budget of 5-6% X, Figure 3.

The stavelet interposer is a thin FPC of Kapton and copper (1-layer but might need 2-layers) to support the sensors and ASIC assembly. As seen in Figure 2 (left), sensors are placed on a large metal pad that provides bias voltage. The ASICs are placed around each sensor they are interconnected via traces going around the sensor on the interposer board, only one of each set of four has external communication with the FPC bus. Sensors and ASICs are glued on the interposer and connected via wirebonds. The interposer board will also host bias capacitor and temperature sensors. Other materials for the stavelet will be explored as well, e.g. thin ceramic (rigid, but higher material budget). Another option is adding stiffeners to the design. The loading tolerance for the sensor is 150um or better to ensure double-sided overlap. A stavelet prototype is shown in Figure 2 (right).

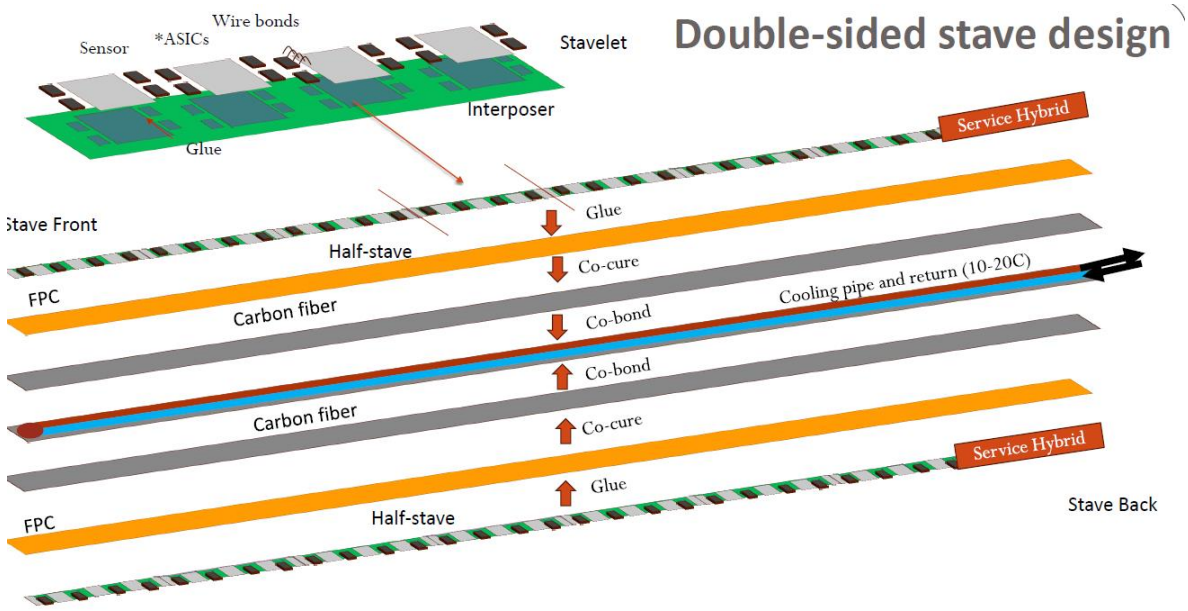

Figure 1. Exploded view of a double-sided stave.

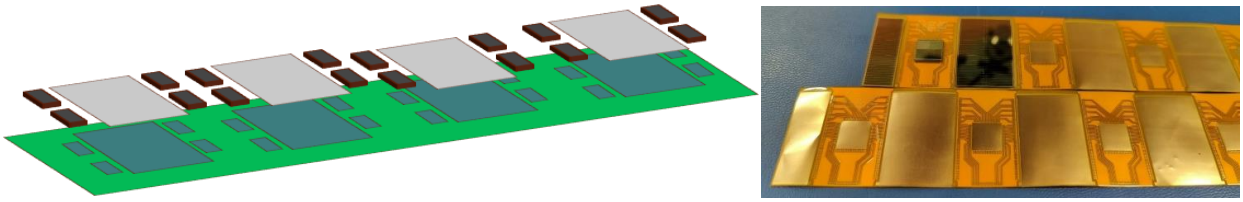

Figure 2. Left: Stavelet components, black: FCFD ASIC, grey: AC-LGAD sensor, green: interposer board. Right: first stavelet prototype fabricated (old design) with some components loaded.

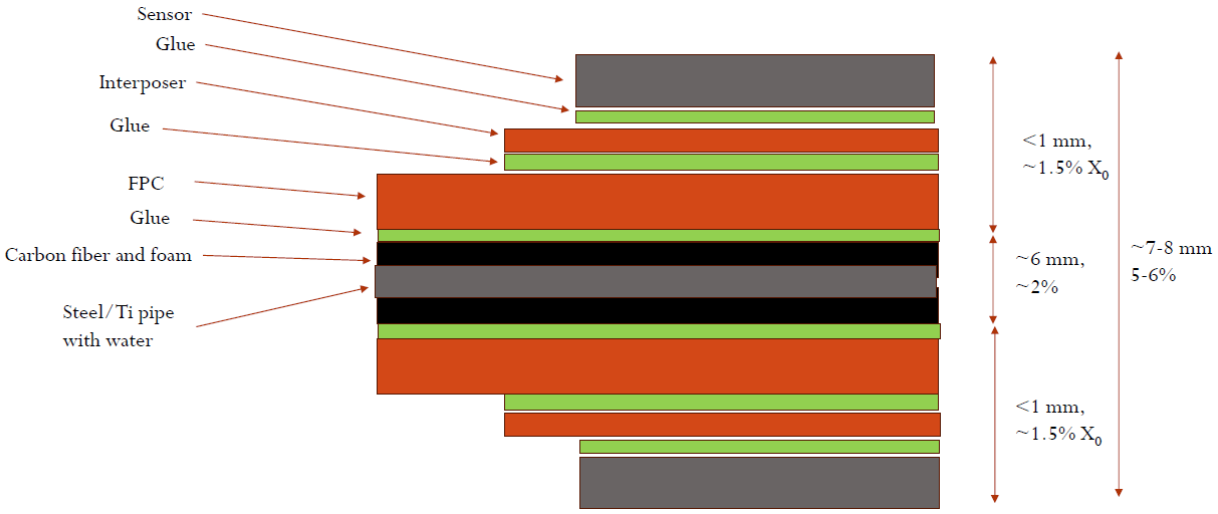

Figure 3. Cross section of a stave stack with thickness and material budget

1.1. Pre-Assembly Parameters

- Workspace, Equipment, and Storage

Parameter	Value
Cleanliness of the assembly area	≥ISO6
Components and stavelet storage requirements	Dry cabinets
Equipment status	Regularly serviced and calibrated
Components	Qualified and certified working
Glue storage	Temperature controlled dry environment

1.2. Post-Assembly Parameters

- Mechanical

Parameter	Value
Mechanical alignment of components	<150um
Measured relative position of components	<5um
Glue thickness	50-100um?
Glue homogeneity	10%?
Glue coverage	>80%?
Connection integrity	Wire bonds pull force >10gF

- Electrical

Parameter	Value
FCFD powering test	Lack of short and open circuits
FCFD digital communication tests	No errors in digital communication
FCFD channel operation	<X%? of bad channels
FCFD power lines voltage variation	<5%
Sensor operation	Breakdown voltage between [180, 190] V

- Full System

Parameter	Value
Charge response of each FCFD channel	Homogeneity within X%

2. PROCESSES AND PROCEDURES

2.1. Pre-assembly: Workspace, equipment and storage

The workspace, equipment and storage of detector modules is standardized and monitored.

- Cleanliness of the assembly workspace: to check that the cleanliness of the workspace is sufficient to handle and interconnect 50 µm thin sensors with interconnection pads of ~100 µm size. Failure to do so would impact on the module production yield.
- Servicing of equipment for electrical interconnection (e.g. wirebonding machines): to check that the equipment used to electrically interconnect the detector modules is reliable and does not develop faults that could lead to major downtime and delays in the production of modules.
- Calibration of power supplies and oscilloscopes: to check that the equipment is reliable to supply and measure electrical currents and electrical potentials.
- Environmentally controlled storage of sensors and FCFD: to prevent deterioration of components after acceptance testing.
- Environmentally controlled storage of glue: to prevent deterioration of glue, it will be dry stored at cool temperature.

2.1.1. Verification Testing

- Cleanliness of the assembly workspace: periodic certification of the workspace to meet ISO6 or higher, following the ISO 14644-1 standard.
- Servicing of equipment for electrical interconnection (e.g. wirebonding machines): periodic servicing and maintenance of the equipment for electrical interconnection (i.e. wirebonding machines).
- Calibration of power supplies and oscilloscopes: periodic calibration of the equipment.
- Environmentally controlled storage of sensors and FCFD: to be store in dry storage units.
- Environmentally controlled storage of glue: to prevent deterioration of glue, it will be dry stored at cool (10-15 C) temperature.

2.2. Pre-assembly: Components acceptance testing

The components and tools required to assemble stavelets require acceptance testing in order to verify their compliance with their individual specifications. This process checks that components are suitable for the production of detector grade modules.

2.2.1. Incoming Inspections or Acceptance Testing

- FCFD acceptance testing: to check that the chips are compliant with detector grade requirements. To be assessed via visual inspection and access to a shared database accessible to everyone containing results of verification tests (e.g. visual inspections and metrology (potentially) and electrical tests) performed at the FCFD QC sites.

- Sensor acceptance testing: to check that the sensors are compliant with detector grade requirements. To be assessed via visual inspection and access to a shared database accessible to everyone containing results of verification tests (e.g. visual inspections and metrology (potentially) and electrical tests) performed at the sensors QC sites.
- Interposer acceptance testing: to check that the interposer is compliant with detector grade requirements. To be assessed via visual inspection and access to a shared database accessible to everyone containing results of verification tests (e.g. visual inspections and electrical tests) performed at the FPC QC sites.
- Epoxy glue acceptance testing: to check that the glue is in date and stored according to the manufacturer's requirements.
- Jigs and tools to be metrology tested via coordinate measurement machines at metrology workshops before deployment. This guarantees compliance with the mechanical tolerancing specified in their related mechanical drawings. To inspect the position of alignment pins, flatness, perpendicularity.

2.3. Post-assembly: Mechanical test: glue coverage and homogeneity

The glue coverage and homogeneity are measured to ensure good thermal connection and wire bonding support

2.3.1. Verification Testing

- Automatic inspection by SmartScope; laser measurement of components planarity
- Sample inspection; separate components and verify glue coverage

2.4. Post-assembly: Mechanical test: Welding integrity of microelectronics interconnects

The welded joints that are required by the electrical interconnects (wirebonds) are responsible for the robustness of the module electrical interconnection.

2.4.1. Verification testing

- Visual inspection by microscope; Impedance tests; Pull/shear tests on interconnects.
- Visual inspection before after (potential) potting

2.5. Post-assembly: Mechanical test: Mechanical integrity and alignment of module components

The welded joints that are required by the electrical interconnects (wirebonds) are responsible for the robustness of the module electrical interconnection.

2.5.1. Verification testing

- Visual inspection by microscope; Impedance tests; Pull/shear tests on interconnects.
- Visual inspection before after (potential) potting

2.6. Post-assembly: Electrical test: sensor electrical test

Verify sensor is working after assembly

2.6.1. Verification testing

- Run a current over voltage test on all sensors on the stavelet (probably sharing one bias voltage line) in a dark enclosure. Compare with sum of current over voltage measurements of all sensors mounted from pre-assembly stage.

2.7. Post-assembly: Electrical test: FCFD powering tests

- Impedance measurements: to check for short circuit and open circuit defects.
- Power consumption measurements: to check that the device operates within the functional limits of its power domains.

2.7.1. Verification Testing

- Impedance measurements: To measure the impedance of the power rail without applying any supply voltage. Measurement performed by probe testing on dedicated interposer pads.
- Power consumption measurements: To set the supply current(s) and voltages(s) to the nominal value(s) and to measure the associated current(s); To repeat the measurement with the supply voltage(s) over-biased and under-biased (e.g. min, max) with respect to the nominal value(s).

2.8. Post-assembly: Electrical test: FCFD digital communication tests

Configuration and register read-back measurements to confirm that the device can be configured and it communicates with the other chips

2.8.1. Verification Testing

- Configuration and register read-back measurements: To configure the device and to measure the power consumption of the device after configuration. To write and read back a known value on a selected register multiple times without errors. To check communication with all FCFD daisy-chained together.

2.9. Post-assembly: Full system test: Charge response of each FCFD channel

- Digital scan to check the response of the in-channel digital circuity and the readout path through the highspeed data links.
- Analogue scan to check the response of the in-channel circuity (analogue and digital) and the readout path through the high-speed data links.
- Threshold scan to check the threshold value of the in-channel comparator and the noise of each pixel in units of electrons.
- Threshold tuning to adjust the in-channel comparator to a certain threshold value with a narrow spread across all pixels.

2.9.1. Verification Testing

- Digital scan: To inject a known number of digital pulses in the in-channel digital circuitry of each pixel. To count the number of recorded hits detected in each pixel.
- Analogue scan: To inject a known number of analogue pulses with fixed amplitude in the in-channel analogue circuitry of each channel. To count the number of recorded hits detected in each channel.
- Threshold scan: To scan the amplitude of analogue pulse from low to high. For each amplitude, to inject a fixed number of pulses in each channel and record the number of detected hits. Perform the first derivative of the obtained S-curve to extract the associated Gaussian. To extract the mean value for threshold measurement, and the standard deviation for the noise measurement.
- Threshold tuning: To scan iteratively the in-channel settings/registers to set the voltage as close as possible to the target value.

- Charge collection: Bias the sensors and inject a known charge in each channel using an X-ray source. Verify homogeneity of channel response.

3. EXPERIMENTAL/TEST SETUPS

3.1. Post-assembly: Mechanical tests

Visual inspections: to be performed via microscopes and/or optical metrology equipment, with possible automation. Position of components on the board in respect of alignment markings measured with <5um precision. Leveling of components to evaluate glue planarity measured with <Xum precision.

Pull/shear tests on interconnects: to be performed with dedicated commercial off the shelf pull/shear test equipment.

3.1.1. Resource Requirements

- Visual inspections: This is a one-person task using a microscope and and/or optical metrology equipment.
- Pull/shear tests on interconnects: This is a one-person task using the pull/shear test equipment.

3.1.2. Resource Test conditions

- Visual inspections: Good lighting conditions, in clean room.
- Pull/shear tests on interconnects: Good lighting conditions, in clean room

3.1.3. Equipment

- Visual inspections: Microscopes and/or optical metrology equipment. Example equipment shown in Figure 4.
- Pull/shear tests on interconnects: pull/shear test equipment.

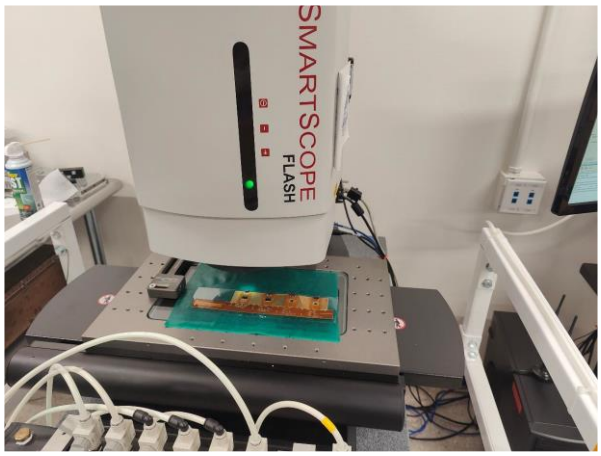

Figure 4. Metrology station (SmartScope) inspecting a mockup stavelet

3.2. Post-assembly: Electrical tests

The assembled stavelets will be tested with a test board (Figure 5) that comprehends a temporary FPC (or PCB), clamped/connected to the interposer board, and a service hybrid. The SH will communicate with a test FPGA that is connected to a DAQ PC for the testing. The DAQ PC will ave automated scripts to run the testing. The schematics of the setup are shown in Figure 6. The FCFD chips will be tested using both internal charge injection from the FPGA and using an external source to inject a known signal inside the

sensors, the source, possibly mounted on a sliding motor, can scan across all four sensors positions on the stavelet.

3.2.1. Resource Requirements

The test system will consist of a custom-made printed circuit board (PCB) for data acquisition (DAQ). This DAQ card will perform readout and control operations on the stavelet. Tests will be automated via scripts running on a PC. The PC will control the peripheral DAQ card and the power supplies. The software of the system will combine a series of scripted scans that will be executed sequentially as part of the qualification tests on the module. Quality factors will be extracted from the tests using fiducial cuts. They will be used to accept or reject modules.

3.2.2. Test conditions

Electrical tests on stavelets will be performed at room temperature and in a dark environment to avoid the undesired noise produced by photo-generated currents. It is under consideration the adoption of a metal cooling plate to support the module during the post assembly qualification tests. The plate will be connected to a chiller with water as coolant.

3.2.3. Equipment

Tests will be automated via scripts running on a PC. The PC will control the FPGA that will control the SH. Schematics are shown in Figure 5 and 6.

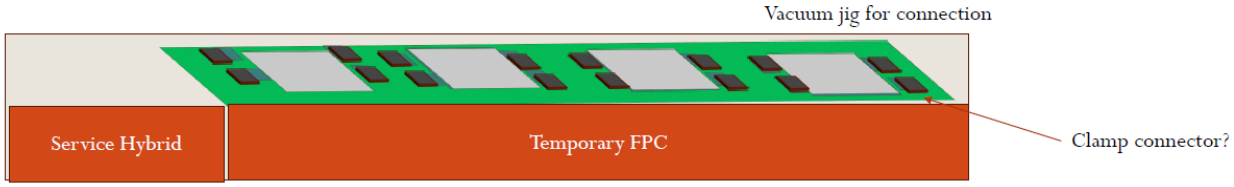

Figure 5. Mechanical schematics of the test board, the setup will be in a dark box

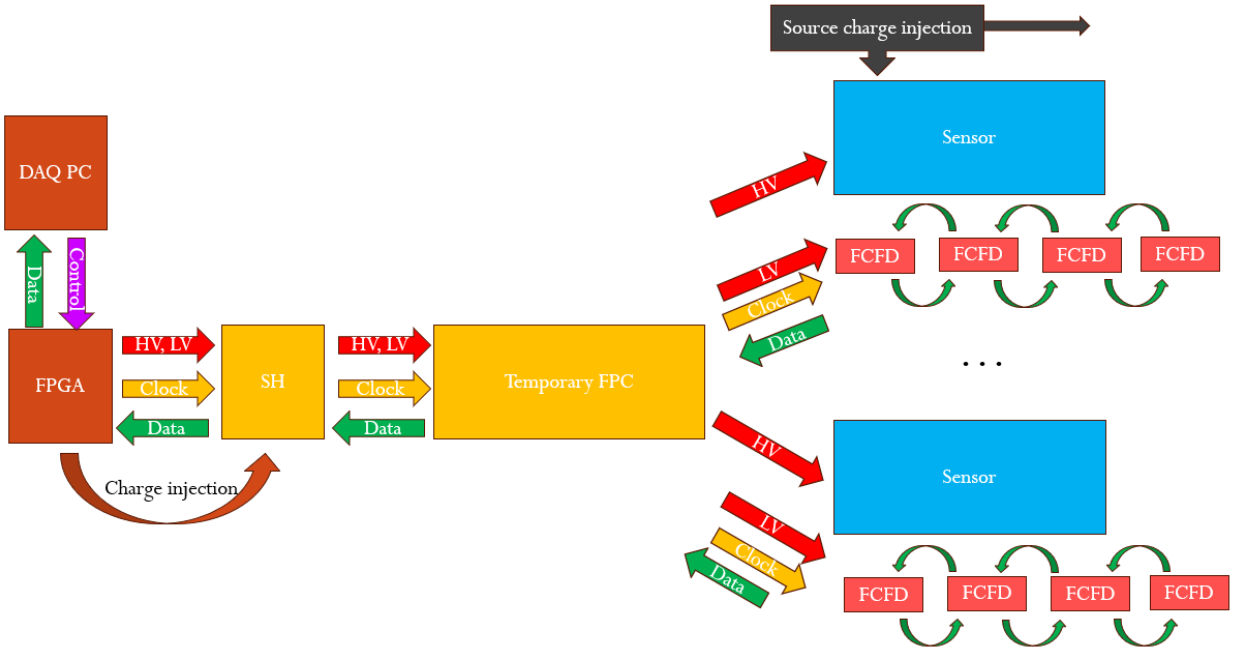

Figure 6. Schematics of the test board, the chips will be tested both with internal charge injection and with charge injection via a source on the sensor.

4. ENVIRONMENT, SAFETY & HEALTH CONSIDERATIONS

All procedures described in this document are carried out in accordance with the Environment, Safety, and Health (ES&H) policies of the relevant laboratories and work areas. Activities are implemented following the established Work Planning and Control frameworks of the participating institutions:

- At University of California, Santa Cruz (UCSC): Activities comply with the university's Environmental Health and Safety (EHS) regulations, ensuring adherence to national regulations for laboratory safety and radiation protection.
- At …: Activities are conducted under the Japan Health and Safety (H&S) policy?
- At Purdue University: Activities comply with the university's Environmental Health and Safety (EHS) regulations, ensuring adherence to national regulations for laboratory safety and radiation protection.
- At Brookhaven National Laboratory (BNL): Work is carried out according to the Integrated Safety Management (ISM), ensuring compliance with U.S. Department of Energy (DOE) regulations and the safe execution of experimental activities.

5. RECORDS AND DOCUMENTATION

Sensors: reports with acceptance tests performed by the responsible sensors QC sites within the BTOF collaboration.

FCFD: reports with acceptance tests performed by the responsible FCFD QC sites within the BTOF collaboration.

Interposer: reports with acceptance tests performed by the responsible interposer QC sites within the BTOF collaboration, and external manufacturers.

Technical datasheets of glues for Control of Substances Hazardous to Health (COSHH). Health (ES&H) policies of the relevant laboratories and work areas. Activities are implemented following the established Work Planning and Control frameworks of the participating institutions:

Documentation: The assembly procedure will be documented in a series of documents, slides or wiki pages as the process gets developed.

Database: A database entry of components (sensor, stavelet, FCFD) proprieties (pictures, current over voltage, digital communication tests, position from Metrology etc.) will be added in database accessible to public. This will allow the collaboration and future reviewers to keep track of all components and assemblies during the installation and run.

6. REFERENCES

EIC Systems Engineering Group. (2022). *Interface Management Plan.* Brookhaven, NY: Brookhaven National Laboratory.

EIC Systems Engineering Group. (2022). *Requirements Management Plan.* Brookhaven, NY: Brookhaven National Laboratory.

EIC Systems Engineering Group. (2022). *Systems Engineering Plan.* Brookhaven, NY: Brookhaven National Laboratory.