CALOROC Quality Control: Tests and Acceptance Criteria

Omega Microelectronics

Abstract

This document is based on the work carried out by the LLR and OMEGA groups on quality checks for the HGCROC and H2GCROC ASICs. Two robots were set up to automate the various tests, depending on whether the chosen package is High Density (HD) or Low Density (LD). Since CALOROC is largely derived from H2GCROC, a significant part of the quality checks will be equivalent and are described in this document.

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1. PRODUCT PROPERTIES

The following are the key properties of the CALOROC that is an Application-Specific Integrated Circuit (ASIC) used for streaming-readout compatible readout of many of the calorimeters in the electron-Proton/Ion Collider (ePIC) detector.

- 1D board, 36 channels
- 130 nm CMOS technology
- Charge (ADC+TOT) + Time (TOA)
- Front end options pending application are either TOT (CALOROC1A) or switched-gain (CALORIC1B), both with the same back end.
- Cdin: 500 pF-10 nF
- Dynamic Range: up to 12 nC
- Timing: <500 ps (1 MIP)
- ADC: 10b; TOT: 15b
- 39.4 MHz operation from BX 98.5 MHz
- Links: 1260.8 Mbps @ 39.4 MHz, multiple
- Power: 10 mW/ch
- Streaming readout compatible
- Radiation tolerant

The CALOROC is based on the earlier HGCROC ASIC that was designed for the High-Granularity Calorimeter (HGCAL) of the Compact Muon Solenoid (CMS) detector and has wide applicability in the CERN Large Hadron Collider and other experiments. HGCROC has to withstand the x100 higher radiation hadron backgrounds of the High-Luminosity LHC experiments as compared to EIC.

2. PROCESSES AND PROCEDURES

2.1. Introduction to the Tests and Robots

The HGCROC quality control process consists of the automatic qualification of approximately 120,000 chips required for HGCAL, including 36,000 HD Si, 84,000 LD Si, and 4,300 LD SiPM devices. To perform these tests, two dedicated robots have been installed at the LLR research institute and OMEGA.

The main requirements of the quality control procedure are that the duration of each chip test should not exceed five minutes, the rate of false positives should remain close to zero, and the results must be stored for long-term accessibility.

Chip qualification relies on a series of tests designed to cover the essential functionalities of the ASIC. These include verifying the ability to power the chip, ensuring reliable communication via the I2C interface, and evaluating the performance of the ADC as well as the TOA/TOT measurements.

The robot installed at LLR (left) is dedicated to the qualification of HD packages, while the robot located at OMEGA (right) is dedicated to LD packages. Each system is capable of testing up to five chips

simultaneously. Since CALOROC is expected to be delivered in an LD package, its qualification will be carried out with the OMEGA setup.

Figure 1. Robots used for qualifying HGCROC HD packages (left) and LD packages (right).

Each ASIC will be labelled with a QR code during the packaging process. An example is given below.

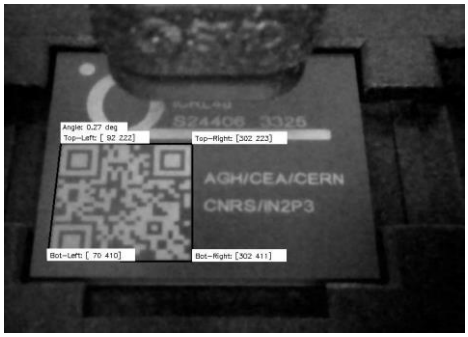

Figure 2. QR code on ASIC package

2.2. Testing software of HGCROC for CALOROC

The testing software used for the qualification procedure is based on the framework originally developed at CERN and OMEGA (CMS restricted: https://gitlab.cern.ch/hgcal-daq-sw/hexactrl-script). This code has been adapted (LLR) for the robots and the modified version is maintained at https://gitlab.cern.ch/evernazz/hexactrl-script/-/tree/robot-2025/.

In addition, a dedicated analysis framework has been developed to extract the relevant parameters, apply the selection criteria for chip qualification, and produce the corresponding plots. This framework, available at https://gitlab.cern.ch/evernazz/hexactrl-script/-/tree/robot-2025/analysis, is fully Python-based and relies on text configuration files to store all threshold values, providing a convenient and flexible setup.

An example is given below where 3 different tests can be seen.

```yaml
power_consumption_run:
    analysis: True
    plots: False
    perchannel: False
    thresholds:
        current_init: [-0.05,0.9] # sometimes the init current is negative since it needs to stabilize
        current_Run0: [0.13,0.37]
        current_Run1: [0.6,0.8]

i2c_run:
    analysis: True
    plots: False
    perchannel: False
    parameters:
        default_config_file: "/home/asictest/HGCAL/robot/hexactrl-script/configs/poweron-default-roc3b.yaml"
    thresholds:
        diff_default: [0,0]
        diff_config: [0,0]

pedestal_run_0:
    analysis: True
    plots: True
    perchannel: True
    nb_max_outliers:
        pedestal: [0, 0] # first below, second above
        noise: [0, 0]
    thresholds:
        pedestal: [0,300]
        noise: [0.9,4.5]
```

Figure 3. Example Testing Code

2.3. Test Structure

The testing logic is structured around the use of boolean flags. Each individual test generates a set of flags, all of which must be set to True in order for the test to be passed. Thresholds are applied to different quantities, such as the raw value of a measurement (e.g. current), parameters obtained from a fit, or the number of outliers. Thresholds are defined and documented in the dedicated configuration files (HGCROC or CALOROC in the future).

Each test also produces “super-flags,” which correspond to the logical AND of the individual sub-flags. A chip is considered qualified only if all of its super-flags are set to True, with no exceptions allowed. Both the measured values and the thresholds applied to them are systematically stored, with a summary YAML file keeping track of all relevant information (see below).

Finally, the test sequence always proceeds to completion, even if a failure occurs at an intermediate step. This ensures that statistics on failing chips are collected consistently across all tests.

```yaml
flags:
  roc_s0:
    slope: true
    offset: true
    chi2: true
    super_pedestal_scan_flag: true
```

```
    chan_71:
      pedestal: 115.59
      noise: 1.23
    calib_0:
      pedestal: 132.23
      noise: 1.08
    calib_1:
      pedestal: 139.12
      noise: 1.05
    cm_0:
      pedestal: 119.36
      noise: 1.12
    cm_1:
      pedestal: 140.31
      noise: 1.13
    cm_2:
      pedestal: 103.94
      noise: 1.06
    cm_3:
      pedestal: 62.57
      noise: 1.05
thresholds:
  pedestal:
  - 0
  - 300
  noise:
  - 0.5
  - 4.5
```

Figure 4. Testing logic for CALORIC to pass quality tests.

3. EXPERIMENTAL/TEST SETUPS

3.1. Power consumption test

The first step in the qualification procedure is the power consumption test. The current drawn by the chip is monitored three times using a controllable power supply unit.

Initial check: This step verifies the absence of a short circuit. The measured current must be below 0.9 A. If this condition is not satisfied, the current_init flag is set to False and the chip will ultimately be rejected.

Run 0: At this stage, the firmware is loaded into the ZYNQ, and the I2C and DAQ servers are initialized. Communication with the chip is established, although the device remains in sleep mode (not yet configured for data taking). The acceptable current range is 0.13–0.37 A.

Run 1: Performed after the I2C test, this step configures the chip through I2C, placing it in data-taking mode. The measured current must then fall within the range 0.6–0.8 A.

The plots for these 3 steps are shown below.

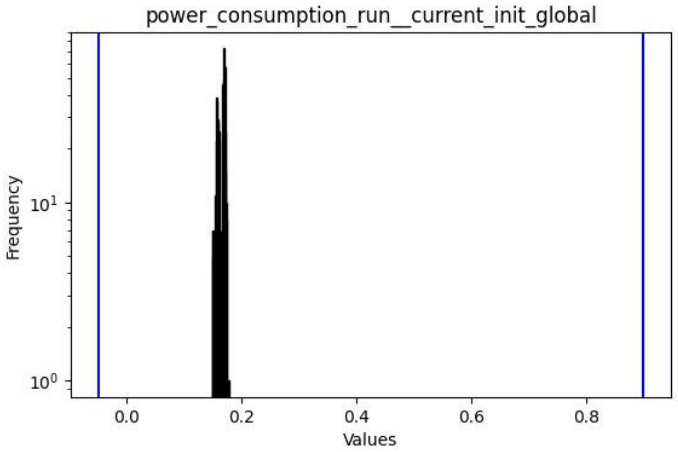

Figure 5. Initial Power Consumption Results

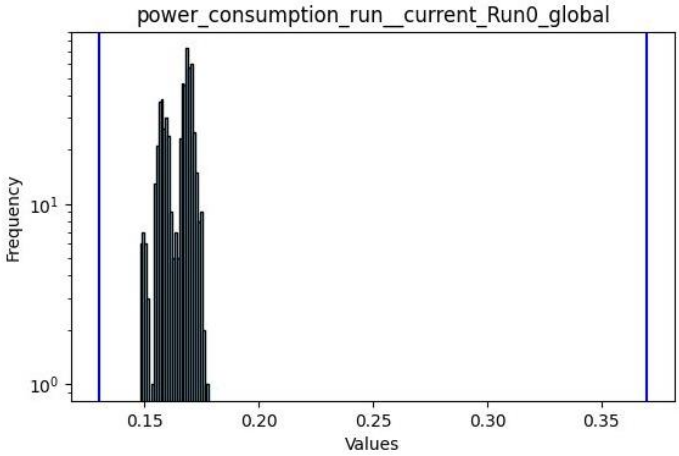

Figure 6. Run 0 Power Consumption Results

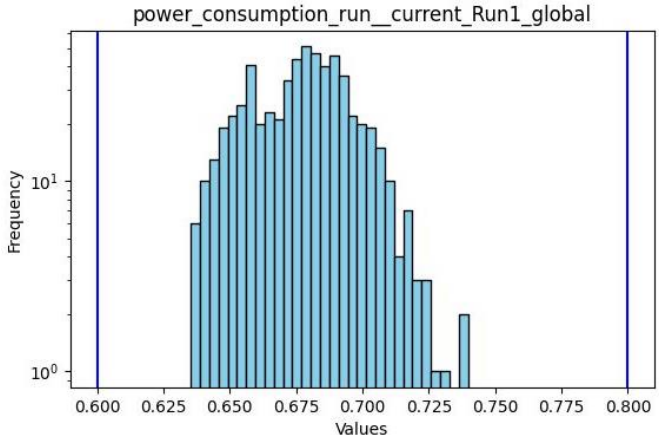

Figure 7. Run 1 Power Consumption Results

3.2. Slow control (I2C) tests

The I2C test verifies that communication with the chip is functioning correctly and that the I2C parameters can be reliably read and written. Initially, all I2C parameters are read from the chip in its default configuration and must match exactly the expected default values. Subsequently, a custom configuration is applied, which inverts all bits of the default configuration (changing 0s to 1s and vice versa) to ensure that all parameter values can be written and read back correctly. Chips that fail either of these checks are identified as non-compliant.

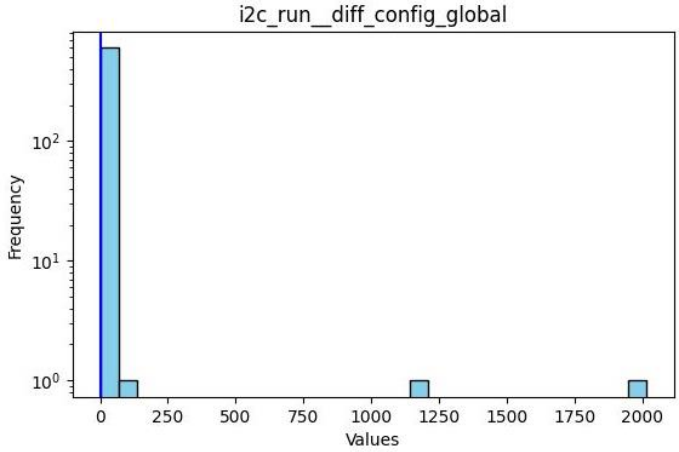

Figure 8. Results of the I2C verification test in default configuration.

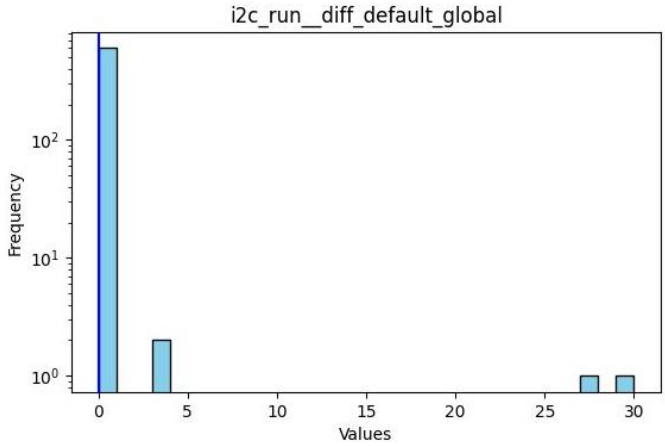

Figure 9. Results of the I2C verification test with all bits inverted.

3.3. Pedestal run checks

Before equalizing the pedestals, an initial pedestal run is performed to evaluate the mean pedestal and the noise for each channel, based on approximately 10,000 events. For every channel, the mean pedestal is required to fall between 0 and 300 ADC counts, with an expected value around 100 ADC. The noise, defined as the RMS of the pedestal distribution, must lie between 0.4 and 4.5 ADC counts, with the setup typically yielding approximately 1 ADC. Channels that are dead or non-functional would generally exhibit zero noise (example below).

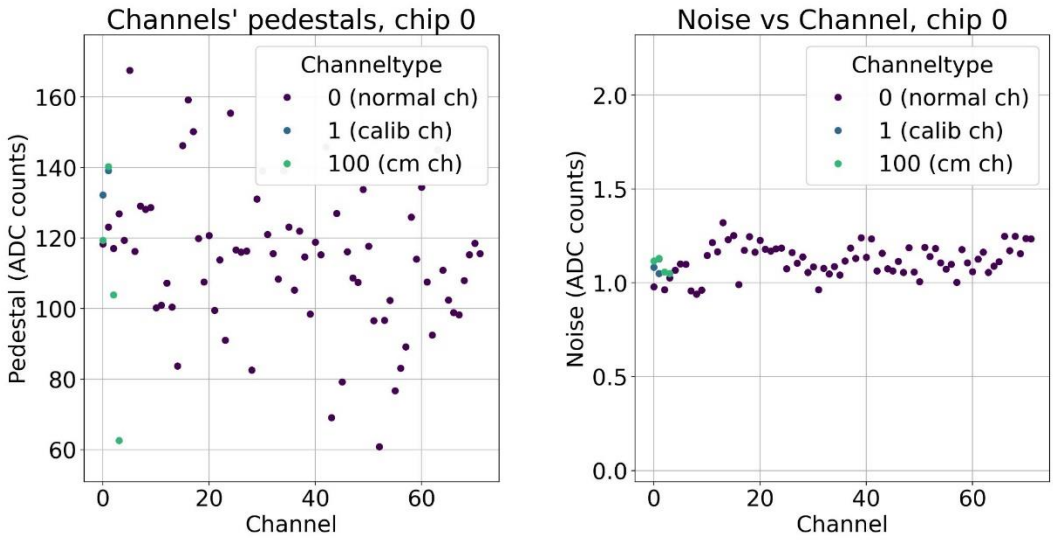

Figure 10. Results to evaluate the mean pedestal and the noise for each channel.

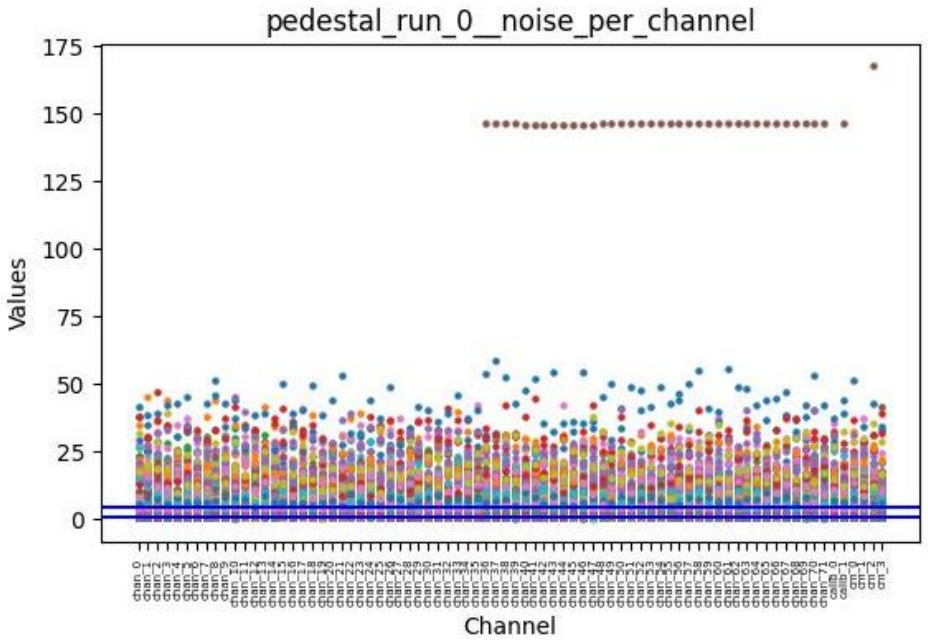

Figure 11. Combined results to illustrate that channels do not exhibit zero noise

3.4. Pedestal scan

The pedestal scan constitutes the first step of the pedestal equalization procedure. This is performed by varying the channel-wise trim inversion DAC. The highest pedestal value measured at trim-inv = 0 across all channels is selected as the target for each half of the chip.

For each channel, a linear fit of the pedestal as a function of the trim-inv parameter is performed to determine the slope and offset.

$$\text{pedestal} = \text{slope} \cdot \textit{trim-inv} + \text{offset}$$

The fit parameters must satisfy the following criteria: the slope should lie between 1.3 and 2, the offset between 0 and 250 ADC counts, and the fit χ^2 must fall within 0 to 20. Once the fits are validated, the pedestal values for each half are equalized according to the measured targets.

A pedestal scan is show below: DAC values are scanned from 0 to 63 to find a common pedestal for all the channels.

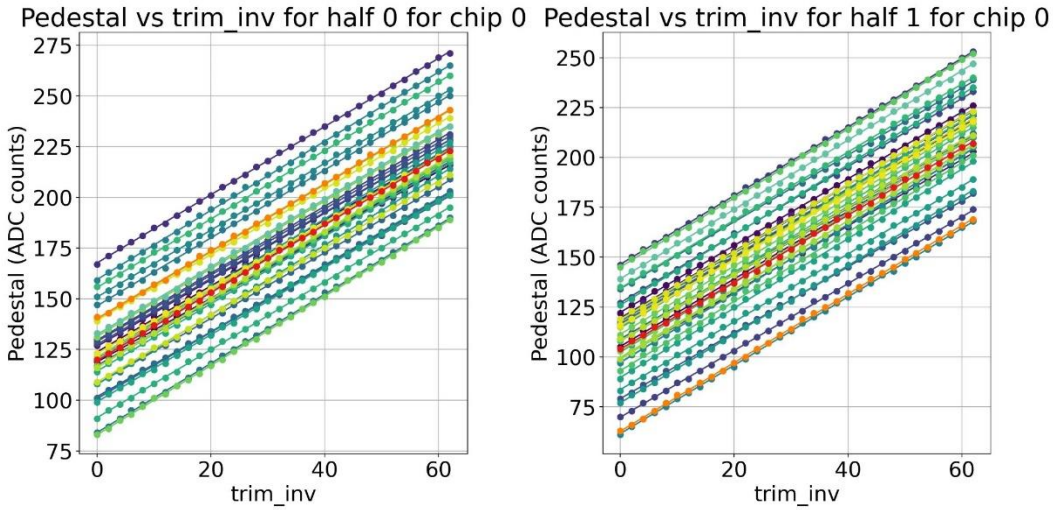

Figure 12. Results of the pedestal equalization process.

3.5. ADC trimming with Vref-inv and Vref-noinv

To bring the pedestal to the desired value, currently set at 80 ADC, the global voltages Vref-inv and Vref-noinv are scanned sequentially for each half of the chip. For one reference channel per half, the pedestal response is fitted linearly as a function of Vref-inv or Vref-noinv.

$$\text{pedestal} = \text{slope} \cdot \textit{Vref-inv} + \text{offset}$$

For every channel, the fit parameters are required to meet the following criteria: for Vref-inv, the slope must be between -1.45 and -1.1, the offset between 800 and 950 ADC counts, and the fit χ^2 between 0 and 20; for Vref-noinv, the slope must lie between -0.6 and -0.2, the offset between 120 and 240 ADC counts, and the fit χ^2 between 0 and 20. These scans allow precise adjustment of the pedestal across all channels.

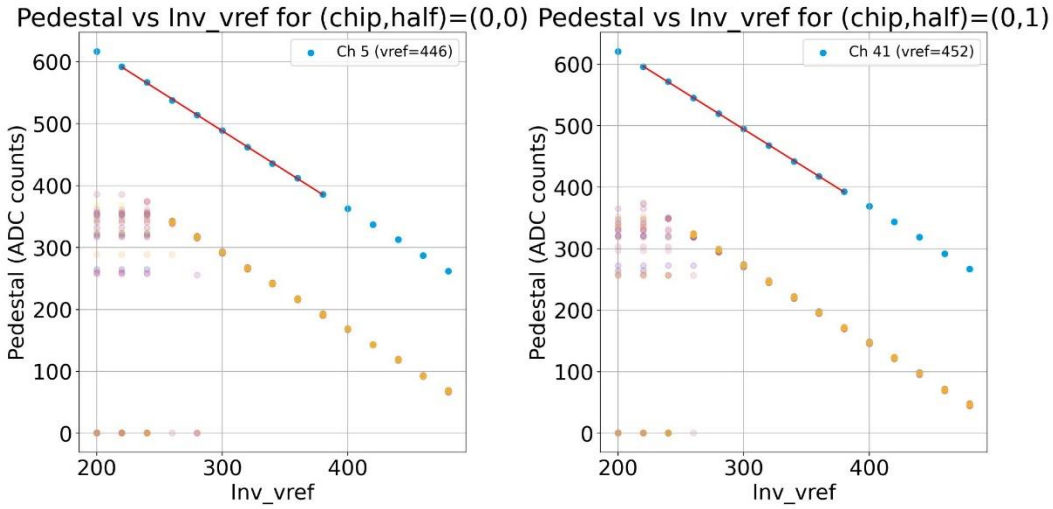

Figure 13. Results of the pedestal reference channel response versus inverted voltage.

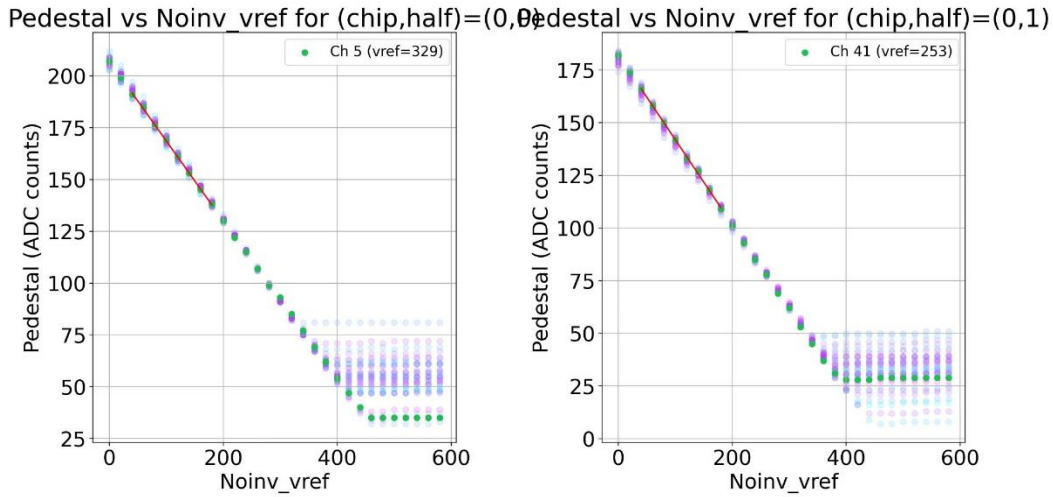

Figure 14. Results of the pedestal reference channel response versus non-inverted voltage.

3.6. Pedestal run adjustment

Following pedestal equalization, an adjusted pedestal run is performed to verify the effectiveness of the procedure. For each channel, the mean pedestal and RMS, which defines the noise, are evaluated over approximately 10,000 events. The mean pedestal is required to lie between 50 and 100 ADC counts, with an expected value of 80 ADC. The noise must be between 0.5 and 4.5 ADC counts, with the setup typically producing around 1 ADC. Channels that are non-functional or dead generally exhibit zero noise.

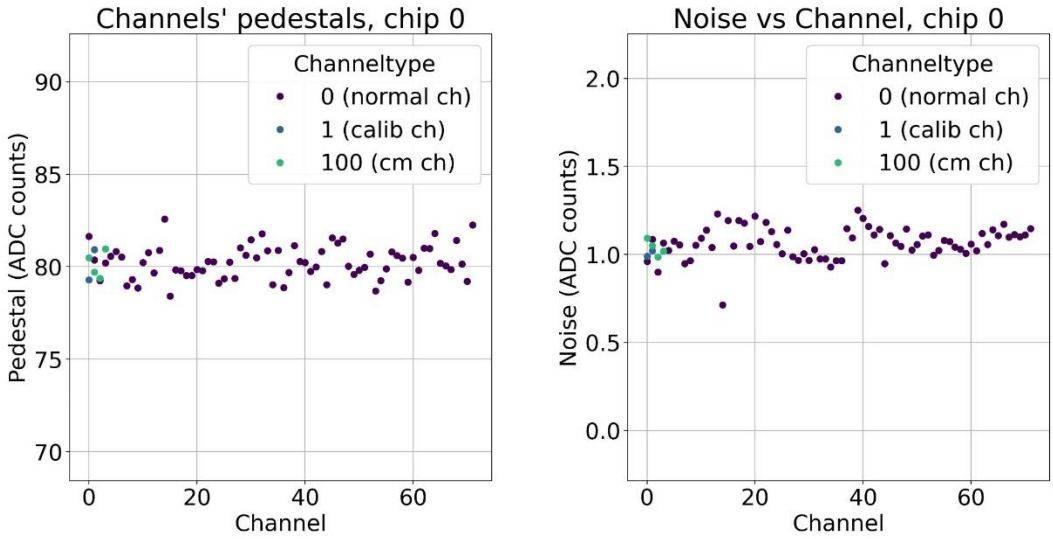

Figure 15. Results of the adjusted pedestal run after equalization.

3.7. Phase scan

The phase scan aims to evaluate the per-channel average pedestal modulation, which can arise due to grounding, and to verify that all channels are properly connected to external sensors. This is accomplished by measuring the expected pedestal modulations caused by clock interference over 16 phases in a selected bunch crossing.

For each channel, the amplitude of the modulation is required to lie between 0.5 and 25 ADC counts, although a per-channel threshold is planned in the future to account for observed patterns versus channel number. The noise is required to fall between 0.5 and 6.5 ADC counts.

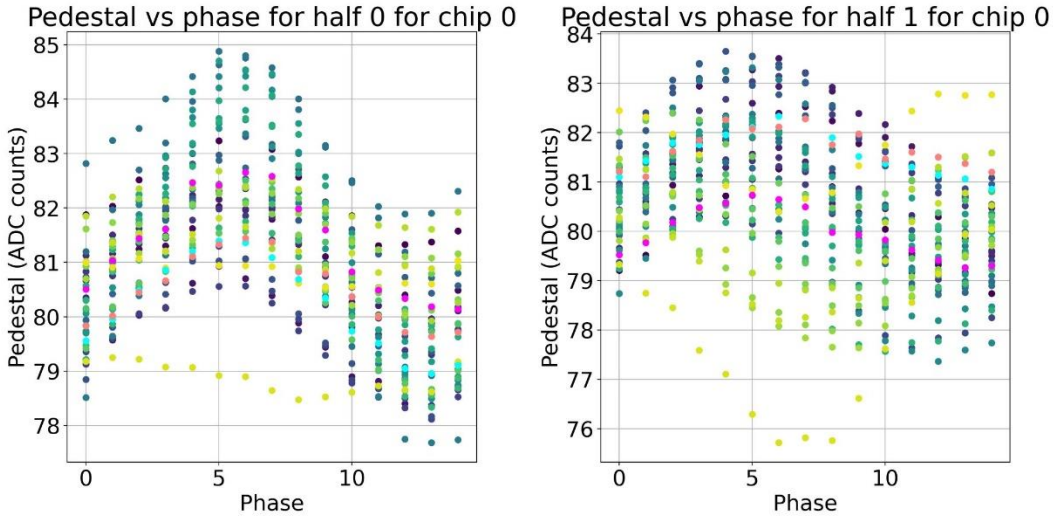

Figure 16. Results of the phase scan showing the per-channel average pedestal modulation.

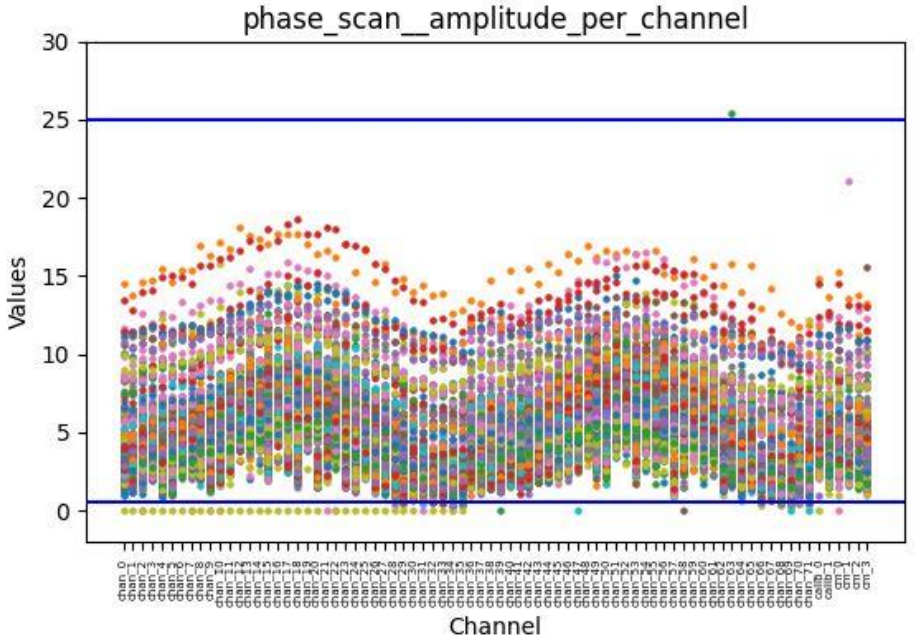

Figure 17. Results of the amplitude of the modulation of the phase scan.

3.8. Sampling scan ADC

A sampling scan is performed using a small charge injection to simulate the signal on the chip. This procedure validates the signal shape, amplitude, and time of arrival (TOA) for each channel. The ADC pulse shape is fitted with a dedicated function, and the resulting parameters are required to satisfy specific criteria.

$$f(t) = A_0\, e^{-aT}\left[e^{-cT}\left(\frac{T^3}{c} - \frac{3T^2}{c^2} + \frac{6T}{c^3} - \frac{6}{c^4}\right) + \frac{6}{c^4}\right]$$

$$T = t - t_0, \quad a = 1/\tau_p, \quad c = 1/\tau_p - 1/\tau_s$$

For each channel, the maximum ADC value must lie between 500 and 700, the phase of the ADC maximum between 0 and 15, and the time of the ADC maximum between 35 and 60. The noise in the following bunch crossing is required to be between 0 and 5, while the shaping time constants τP and τS must be within 8–14 and 0.2–0.45, respectively. The baseline offset t_0 must be between 28 and 34, and the fit χ^2 is required to fall within 0 to 0.3. These measurements ensure that the pre-amplifier and shaper characteristics meet the expected performance.

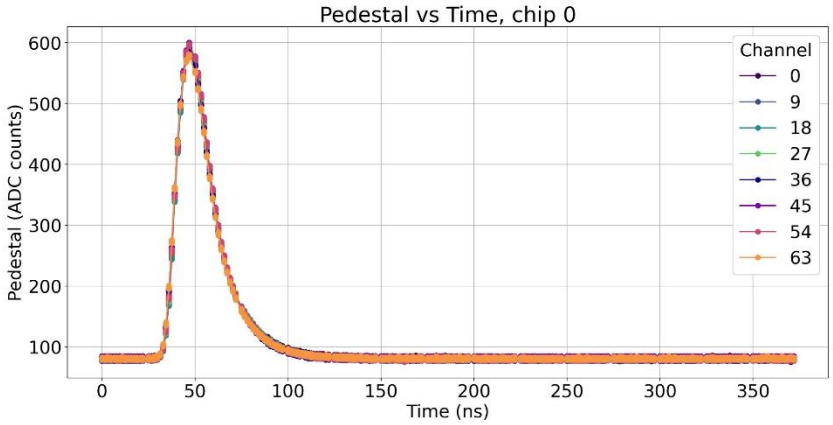

Figure 18. Results of the sampling scan of the ADC.

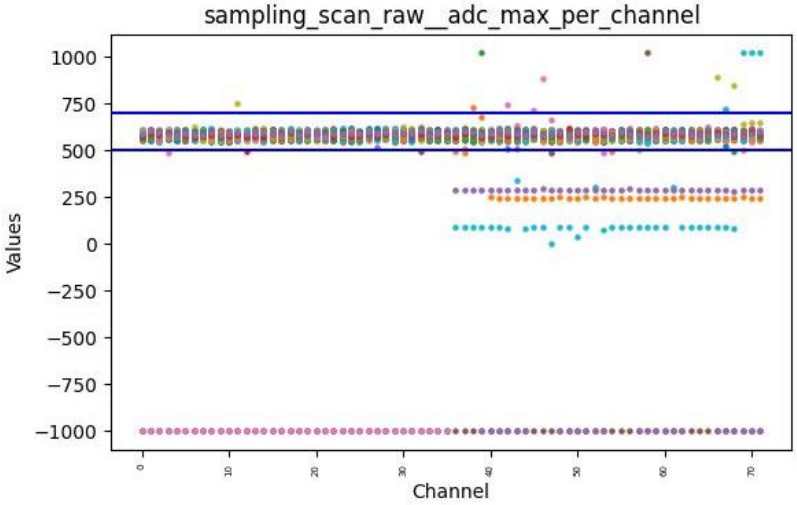

Figure 19. Results of the maximum ACD value for each channel.

3.9. Sampling scan TOA

In addition to the ADC pulse measurement, a sampling scan of the time of arrival (TOA) is performed using a small charge injection to simulate the signal on the chip. This test validates the TOA characteristics for each channel.

For every channel, the TOA response is fitted with a dedicated function, and the resulting parameters are required to meet specific criteria.

$$\mathrm{TOA} = \mathrm{slope} \cdot \mathrm{time} + \mathrm{offset}$$

The TOA maximum must lie between 750 and 1024, its phase between 0 and 15, and the time of the TOA maximum between 35 and 60. The noise in the following bunch crossing must be between 0 and 5, while the slope is required to fall within -60 to -25, and the offset within 1700 to 2500. These measurements ensure that the timing response of the chip meets the expected performance.

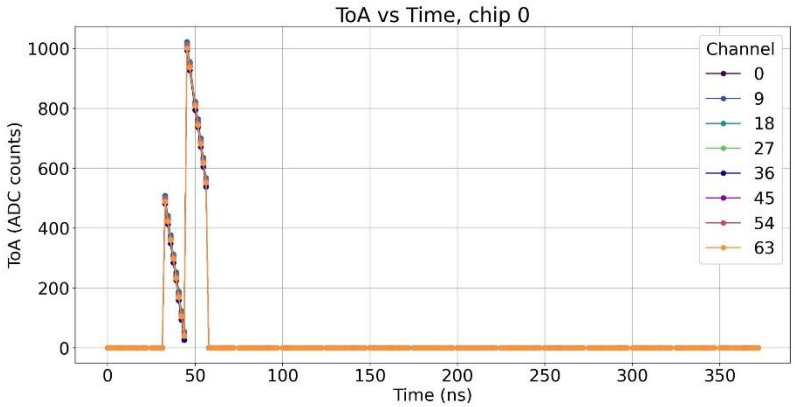

Figure 20. Results of the sampling scan of the time of arrival (TOA).

3.10. Gain scan

The goal of the charge injection scan is to evaluate the gain and linearity of the charge measurement, as well as the behavior of the time measurement across the full dynamic range. Charge is injected into both the ADC and TOT regions, and measurements of ADC, TOA, and TOT are recorded for all channels. Due to timing constraints, only two charge levels are used, corresponding to calibration DAC values of 1000 and 3095. These values are complementary, ensuring that all DAC bits can be configured. In low-range and high-range modes, the charges are injected into the 0.5 pF and 10 pF capacitances, respectively.

The test is also repeated with trim-TOA and trim-TOT set to 63 (all bits on), allowing verification that the trimming DACs for TOA and TOT thresholds can be properly configured without performing long s-curve measurements. Efforts are underway to further assess linearity by adding additional points within the ADC and TOT ranges. For example, adc_1000_0_0 corresponds to DAC = 1000, low-range, trim TOA/TOT = 0, while tot_3095_0_63 corresponds to DAC = 3095, low-range, trim TOA/TOT = 63.

In addition to the functional and timing tests, two additional flags are monitored for each channel to ensure data integrity. The unvalidtp flag, returned by the unpacker, is non-zero if the trigger links are not aligned and is required to be zero for proper operation. Similarly, the corrupted_events flag, also returned by the unpacker, indicates misalignment of the data links and must likewise be zero. These checks ensure that both trigger and data paths are functioning correctly.

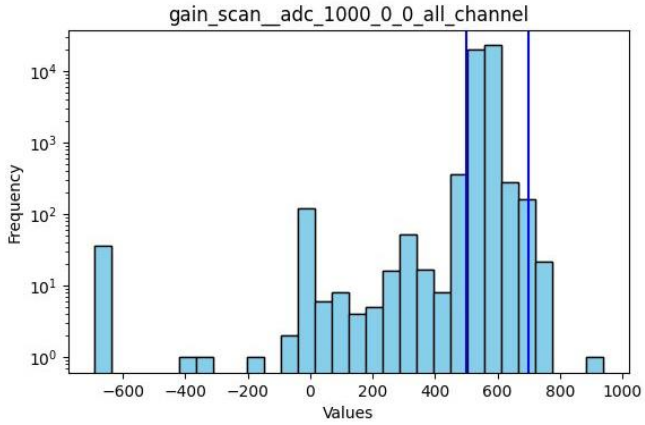

Figure 21. Results of the gain scan of the charge measurement.

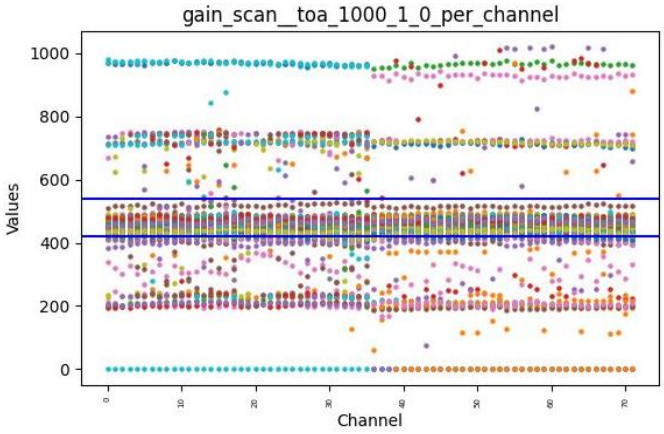

Figure 22. Results of the gain scan of the time measurement.

3.11. Yield

The yields are systematically monitored throughout the testing procedure. In the calculation of these yields, misplaced chips—that is, chips for which data-taking could not be completed due to crashes or other interruptions—are excluded from the statistics.

In 2025, with the production of a large number of HGCROC chips, an overall yield of 80% was achieved. The top picture shows the results from the testing of more than 4000 ASICs, while the bottom picture corresponds to over 10000 LD chips.

The overall estimated yield is folded a priori into the EIC detector project procurement process.

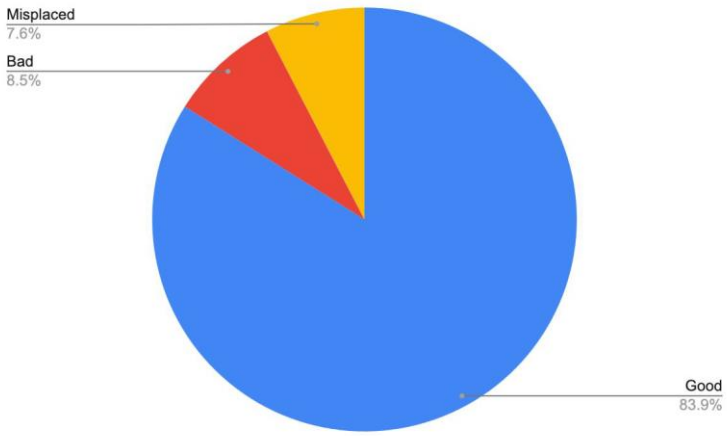

Figure 23. Example of the systematic monitoring of the yield of 4000 ASICs.

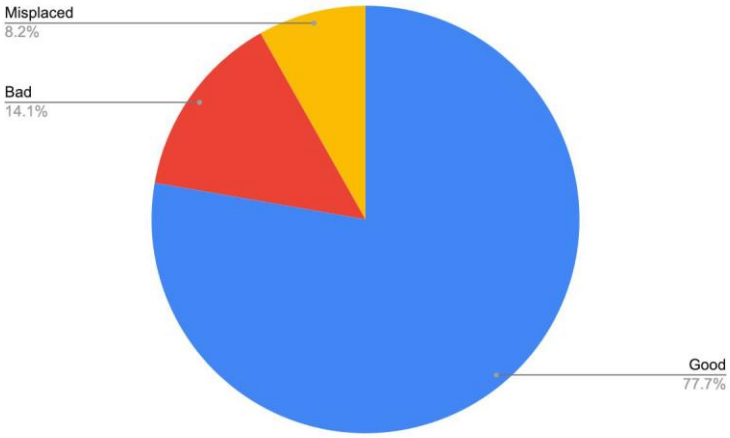

Figure 24. Example of the systematic monitoring of the yield of 10000 LD ASICs.

4. ENVIRONMENT, SAFETY & HEALTH CONSIDERATIONS

The procedures will be implemented in a way consistent with the environment, safety, and health policies of the relevant work areas. Within Jefferson Lab the process is described in the ES&H manual Chapter

3200, Work Planning and Control Program and at BNL within the SBMS: “Work Planning & Control for Experiments and Operations”.
For this work no specific personal protection equipment and materials are used:

5. RECORDS AND DOCUMENTATION

This section details all of the documentation that will be generated and exchanged during the manufacturing lifecycle. In all likelihood there will be many transient documents that are created that will not be collected or maintained as part of the project. This transient documentation need only be listed if it is pertinent to a specific experiment or test.

5.1. Manufacturer/Producer Records

For every item that is manufactured, the manufacturer will be responsible for maintaining records (travelers) of all raw material that are used in the fabrication process, and document the processes and procedures that were used for production. The resultant documentation will be compiled into a report and will be provided to the project as part of the deliverable, which will be reviewed, validated, and then placed in the central data repository.

For CALOROC there are no pertinent manufacturer/producer records of relevance as the quality tests will be done by our ePIC collaborators following the tests described above. Each CALOROC will have a QR code that links them to the various quality tests. The quality tests will ensure that the yield of good-quality CALOROC ASICs is consistent with the assumptions made in the procurement process which is anticipated to be through an in-kind contributor.

5.2. Deliverable Documentation and Records

This includes test results, tables of measurements, parameter lists or other records that must be provided to the project. All testing and inspection data that is collected as part of the validation, verification and testing plan will be provided to the project as part of the final report.

The deliverable documentation follows the examples of inspection tests provided in this document, where the results were based on the HGCROC ASIC which is a predecessor of CALOROC. A final copy will serve as final documentation of the CALOROC ASICs including their QR codes that serve as the traveler during the inspection process. It will include all the tests of CALOROC parameters that are measured.

6. REFERENCES

EIC Systems Engineering Group. (2022). *Interface Management Plan.* Brookhaven, NY: Brookhaven National Laboratory.

EIC Systems Engineering Group. (2022). *Requirements Management Plan.* Brookhaven, NY: Brookhaven National Laboratory.

EIC Systems Engineering Group. (2022). *Systems Engineering Plan.* Brookhaven, NY: Brookhaven National Laboratory.