FLX-155 Inspection and Test Plan

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Abstract

The FLX-155 is a PCIe card based upon the AMD Versal Premium XCVP1552-2MSEVSVA3340 FPGA. It uses Samtec FireFly optical transceivers to provide data transfers from detector electronics and PCIe to connect to DAQ computers. This testing plan ensures that all features of the board perform correctly making use of the Built in Self-Test (BIST) features of the board. The tested components are the fiber interfaces, the PCIe bus, and FPGA components and their interfaces. The testing activity requires both in-process activity by the vendor during construction as well as acceptance testing.

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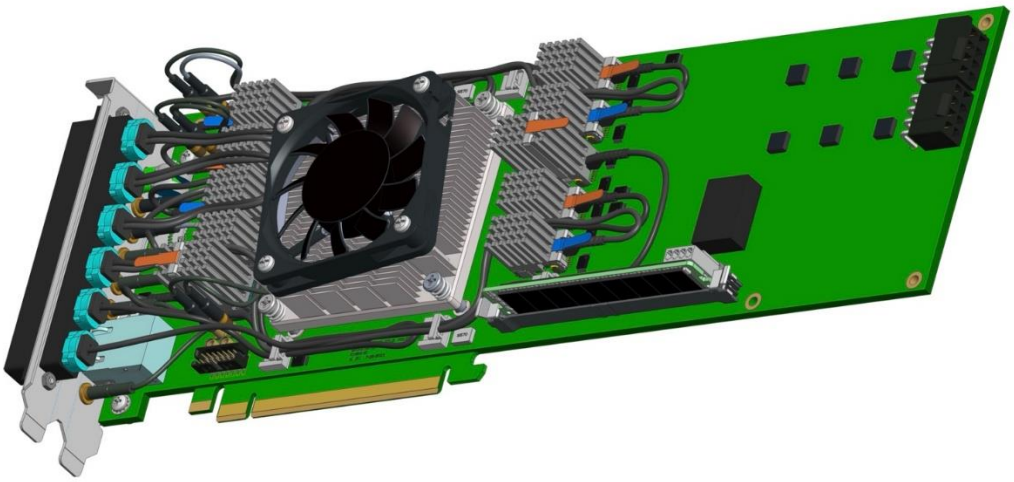

Figure 1. CAD drawing of FLX-155 with the maximum number of optical transceivers installed

The FLX-155 boards are FPGA-based full-height, full-length, double-wide x16 PCIe form-factor electronics boards. The EIC Project will provide the contractor the printed circuit boards (PCBs) and all other electrical components to populate the board including the FPGAs, and Optical Transceivers.

The deliverables consist of the fully assembled electronics boards. Functionality is primarily evaluated using a series of Built In Self Tests (BIST). The results of these test evaluate the proper function of the FPGA, the behavior of the fiber interfaces, and the behavior of the PCIe interface.

2. PROCESSES AND PROCEDURES

The Contractor is required to perform a series of tests during the production of the boards. On delivery, acceptance testing will be performed at BNL.

2.1 Functional Testing

The functionality of the FLX-155 board requires physical coherence of the PCB board at varying temperatures, proper electrical connectivity as evaluated by flying probe tests, the ability to program components including the ADM1266 power sequencer, the FPGA, and QSPI. Once the programmability of the board is verified it is capable of running its own self-tests, making use of loopback dongles on the MTP couplers and PCIe interface, as well as a network interface a computer displaying a web browser. These tests evaluate the interfaces and the internal memory and processing of the board. Results can be visualized on the web browser and are saved to JSON format. Multiple tests can be run in parallel on different browser tabs.

2.1.1. In-Process Testing

The Contractor shall perform Factory Acceptance Tests (FAT) which shall include:

- Thermal cycling of the assembled PCB (unpowered, prior to the installation of mechanical components) compliant to the standard IPC9701A and defined as follows:

    - Temperature range: 0 °C to +60 °C;
    - Temperature rate of change: ~8 °C/minute;
    - Dwells at temperature extremes: 30 minutes;
    - Number of cycles: 10;
- Flying probe on the power rails to verify the absence of shorts and the correct resistance of the main resistors;
- Programming of the ADM1266 power sequencer via I2C interface. After programming, the rail status shall be read back and checked. Task duration: 3 minutes;
- FPGA and QSPI memory programming test via JTAG. Task duration: 5 minutes;
- Built-in self-test. Loopback dongles must be connected to the MTP couplers, and network interface must be connected to a router or switch. The test is run using an internet browser on a computer connected to the same network. The test runs for about 5 minutes;

Test results shall be collated by the Contractor and be included in the FAT report. EIC project personnel, or a representative of its choice, may attend any tests carried out outside the BNL. The Contractor shall notify the EIC project in writing at least ten working days before the proposed date for any such joint tests.

2.1.2. Acceptance Testing

The Site Acceptance Test (SAT) will be performed at BNL by EIC Project personnel on all received cards. The SAT procedure includes:

- Visual inspection
- Re-run of the BIST.

2.1.3. Verification Testing

The FLX-155 is a general board used in the readout chain of every detector. The results of the BIST in the FAT and SAT will verify the performance of each FLX-155 board. The performance of the FLX-155 in full chain readout will be performed as software, and detector components become available. These chains are designed with the capabilities of the FLX-155 in mind, and the results of the full-chain testing do not affect the QA/QC status of the FLX-155 boards.

2.1.4. Failures and Non-Conformances

Samples for which the FAT and SAT results are not compatible will be diagnosed at BNL. If the fault is ascribed to an assembly defect the sample will be returned to the Contractor for replacement alongside a written report.

In case of unrepairable cards because of wrong or poor assembly, the replacement will be done at the Contractor's expense. In case a component provided by the EIC Project is out of local stock, it will be procured and furnished by EIC Project and charged to the Contractor.

The Contractor warrants that the assembly of electronic cards shall be free from defects in workmanship for a period of two (2) years from the date of production. In the event of a failure due to defects in the assembly of the card within the warranty period, the contractor shall repair or replace the defective card, provided that the failure is determined to be a result of such defects in assembly. The warranty does not cover failures or malfunctions of individual components that were properly assembled, regardless of the cause of the component's failure. Additionally, the Contractor shall not be liable for any damages arising

from failures unrelated to defects in the assembly process. To claim under this warranty, the EIC project must document and provide evidence of the defect in the assembly of the card and submit such evidence to the contractor within the warranty period.

3. EXPERIMENTAL/TEST SETUPS

3.1. In-process tests by Contractor (FAT)

The contractor is required provide the capability to performing the thermal cycling of the unpowered PCB boards, and to conduct the flying probe tests. The EIC project will provide the appropriate technical files for conducting the flying probe tests. The EIC project will also provide items to test the boards including:

- MTP24 and MTP12 loopback dongles required for BIST;
- PCIe loopback card required for BIST;
- Aardvark I2C/USB interface for ADM1266 power sequencer programming

3.1.1. Resource Requirements

- **Thermal Cycling**: The contractor must have access to the temperature chambers and sensors to conduct the thermal cycling of the PCB to the standard IPC9701A.
- **Flying Probe Tests:** The contractor must have access to a flying probe test machine
- **AMD1266 Programming:** EIC Project provided Aardvark I2C/USB programmer
- **FPGA and QSPI programming:** The contractor must have access to JTAG cable
- **Built in Self Test (BIST):** EIC Project provided loopback devices

3.1.2. Test Conditions

- Thermal Cycling:
  - Temperature range: 0 °C to +60 °C;
  - Temperature rate of change: ~8 °C/minute;
  - Dwells at temperature extremes: 30 minutes;
  - Number of cycles: 10;
- **Other tests:** room temperature

3.2. Acceptance tests (SAT)

The acceptance tests will consist of visual inspection and running the Built in Self Tests at BNL for each board.

3.2.1. Resource Requirements

- **Built in Self Test (BIST):** loopback devices and web browser enabled computer

4. ENVIRONMENT, SAFETY & HEALTH CONSIDERATIONS

The board should be able to be powered up on the table-top for testing. It only requires low voltage DC power (12 V) and does not have to be plugged into a PCIe slot. This typically does not constitute an ES&H hazard.

5. RECORDS AND DOCUMENTATION

A label reporting a unique numeric identifier shall be placed on each assembled FLX-155. The results of all tests shall be labeled according to the numeric identifier.

Table 1. EIC project will provide the following technical documentation (section 6)

File Name	Description	Version
Schematics/IO1917_1A_schematics.pdf	Schematics	1A
AssemblyDrawing/IO1917_1A_Fab_Drawing_20250626.pdf	Fabrication Drawing	
BOM/IO1917_1A_BOM_RFQ.xlsx BOM/MechanicalComponents.xlsx	Bill of Materials	1A
PasteMask/SolderPasteTop.gdo PasteMask/SolderPasteBottom.gdo	Paste Mask	1A
XYPosition/IO1917_1A_XY_vb_ais.txt	Pick & Place	1A
IO1917_1A.ipc	Netlist for PCB testing	1A
GerberAssembly/*	Gerber Files	1A

5.1. Manufacturer/Producer Records

Printed circuit boards (PCBs) will have manufacturing identifiers. The QA records for each board will indicate that they passed manufacturing continuity testing. Completed FLX-155 boards will be labeled with a unique ID used to tag all FAT and SAT tests. The source of all commercial off the shelf (COTS) components must be identified. The components shall be assembled and installed to a specified industry standard (e.g. Commercial, Ruggedized, Aerospace, etc.)

5.2. Deliverable Documentation and Records

The deliverable documentation will consist of:

- A Factory Acceptance Test (FAT) as defined in section 2.1.1 for each FLX-155 labeled according to its unique identifier. This includes output from the thermal cycling tests, the Flying probe tests, the rail status read back of the ADM1266, and the output of all BISTs.
- The Site Acceptance Test (SAT) as detailed in section 2.1.2 for each FLX-155 labeled according to its unique identifier. The output of all BISTs.

6. REFERENCES

Technical documentation : https://cernbox.cern.ch/s/0WTBF50PSrQTMLn