GTU Inspection and Test Plan

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Abstract

The GTU is a 4U tall, 19" rack mounted box based upon the AMD Ultrascale plus XCZU19P and XCKU15P SOMs. It supports 4x10G QSFP modules and Samtec FireFly optical transceivers to provide clock/controls interfaces between the GTU and up to 148 DAM boards. There is copper gigabit ethernet for Run control interfaces and SMA connectors to interface with the EIC Common Platforms. This testing plan ensures that all features of the GTU perform correctly making use of the firmware features and a high-bandwidth oscilloscope. The tested components include the fiber interfaces, the copper interfaces and the FPGA components and their interfaces. The testing activity requires in-process activity by the vendor during construction, the PCB acceptance testing, GTU built in testing after GTU box assembly and system testing after installation.

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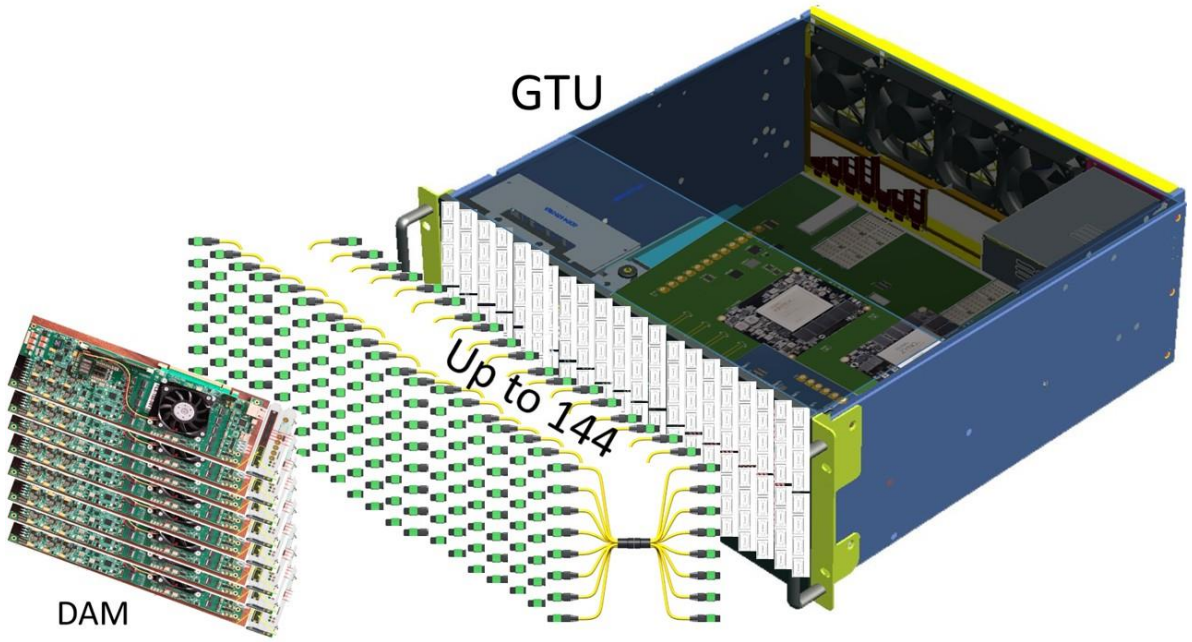

Figure 1. Drawing of GTU with the maximum number of optical transceivers installed

The GTU is an FPGA-based 4U height, full-width 19" rack-mounted, 12" depth box. The GTU box consists of the GTU base board, Optical transceiver plug in boards, cooling fans, and a standard ATX power supply. This GTU box looks like a rack mounted server in format. The EIC Project will provide the assembly contractor with the printed circuit board designs (in electronic format) and all the electronics components to populate the boards. We will have the box's front panel and back panel machined based on our design. We will purchase the AMD Ultrascale plus SOM modules, the Optical Transceivers (the QSFP modules and the Firefly modules), the ATX power supply, and cooling fans separately, and we will assemble the final GTU box in house.

Vendors will produce PCBs and install electrical components for both the GTU base board, and for the optical transceiver boards. These procurements require the same testing.

The final assembly will be done in house, and the functionality testing will be done in house after the final assembly. Functionality is primarily evaluated using a series of Built In Self Tests (BIST) with external fiber cable loop-backs and many test points with a high bandwidth oscilloscope checking for electrical signal integrity. The results of these tests evaluate the proper function of the FPGAs, the behavior of the fiber interfaces and the quality of the electrical signals.

2. PROCESSES AND PROCEDURES

The vendors are required to perform a series of tests during the production of the bare PCB boards and the PCB assemblies. On delivery of the assembled PCBs, acceptance testing will be performed at Jefferson

Lab. After final assembly in Jefferson Lab, additional GTU testing will be performed at the lab before shipment to BNL. Final integrated system testing will be performed at BNL during installation.

2.1 Functional Testing

The functionality of the GTU boards requires physical coherence of the PCB boards at varying temperatures. Proper electrical connectivity is evaluated by flying probe tests dictated by the industrial standard IPC6012 (qualification and performance specification) certificate for bare PCBs, and IPC-A-610, class 2 for PCB assembly. The vendor should be ISO9001 certified (quality assurance and customer satisfaction).

The ability to program components including the ADM1266 power sequencer, the FPGA and QSPI must first be established. Once the programmability of the board is verified, it can run its own self-tests making use of loopback dongles on the MTP couplers and PCIe interface. The user can test the GTU via a web-based application and a network interface. These tests evaluate all interfaces, the internal memory and processing of the board. Results can be visualized on the web browser and are saved to JSON format. Multiple tests can be run in parallel on different browser tabs.

2.1.1. In-Process Testing

The PCB manufacturer and PCB assembly vendor shall perform Factory Acceptance Tests (FAT) which shall include:

- Flying probe on the bare PCBs to verify the absence of shorts, the proper continuity, and different signals isolations.
- Visual inspection of the assembled PCBs, either automatically or manually.

2.1.2. Acceptance Testing

The Site Acceptance Test (SAT) will be performed by EIC Project personnel on all received PCBs. The SAT procedure includes:

- Visual inspection.
- Power delivering tree short check before powering up. Checking of voltage levels and current consumption after powering up will be performed.

2.1.3. GTU testing after final assembly in Jefferson Lab

The GTU (both base board and the optical transceiver plug in cards) will be assembled into the 4U 19” rack mounted chassis. After the final assembly, the GTU box will be checked by the multi-meter: resistance before powering up and voltage and current (voltage drop over resistors) after powering up. The distributed clock quality (signal amplitude, rising/falling times, jitter, and phase stability) will be sample tested via the oscilloscope.

The FPGA SOM modules will be reprogrammed (reloaded) with ePIC firmware. Every optical transceiver will be tested via MTP loopback using their built-in I2C interfaces. These tests will be performed via a software application.

2.1.4. GTU box burn-in test at Jefferson Lab

To mitigate potential “infant” mortality, the GTU box will be tested at an elevated environmental temperature (20 degree Fahrenheit higher than the expected ambient room operating temperature) for

an extended period (~30 days). During the burn-in test, the QSFP parameters will be readout, the GTU power consumption and temperature will be monitored, along with periodic functional tests.

2.1.5. GTU testing after installation in BNL

The GTU box will be shipped to BNL for installation in the DAQ room at IP6. After installation, the GTU will be functionally tested using the actual DAM boards and EIC common platform electronics. These system tests will include the MTP fibers between the GTU and the DAM boards as well as full chain testing with detector sub-system components (RDOs and Front-End Boards).

2.1.6. Failures and Non-Conformances

If any problem (or error) is found during the acceptance testing at Jefferson lab, the defective PCBs will be diagnosed to pinpoint the problem, and the PCBs will be sent back to the manufacture to be repaired (as per warranty). In case of unrepairable cards because of incorrect assembly or poor bare PCB or the replacement will also be done at the vendor's expense (as per warranty).

The GTU testing after final chassis assembly may also find issues. If any problems are found the GTU box will be debugged and repaired at Jefferson Lab. If the problem is a result of faulty FPGA SOM modules, the problem SOM will be shipped back to the manufacturer/distributer for warranty replacement.

Standard vendor warranties state the assembled PCBs shall be free from defects in workmanship for a period of one (1) year from the date of delivery. In the event of a failure due to defects in the bare PCB manufacturing or the assembly of the card within the warranty period, the contractor shall repair or replace the defective card, provided that the failure is determined to be a result of such defects in the bare PCB or the assembly. The warranty does not cover failures or malfunctions of individual components that were properly assembled, regardless of the cause of the component's failure. Additionally, the contractor shall not be liable for any damages arising from failures unrelated to defects in the assembly process. To claim under this warranty, the EIC project must document and provide evidence of the defect in the assembled PCBs and submit such evidence to the vendor within the warranty period.

3. EXPERIMENTAL/TEST SETUPS

3.1. In-process tests by Contractor (FAT)

The contractors are required to provide the industry standard certifications for both the bare PCBs and the assemblies.

3.2. Acceptance tests (SAT)

The acceptance tests will consist of visual inspections and running the Built in Self Tests (BIST) at Jefferson Lab for each board.

3.2.1. Resource Requirements

- **Built in Self-Test (BIST):** loopback devices, network and web browser enabled computer
- **Multi-meter and high-bandwidth oscilloscope**

4. ENVIRONMENT, SAFETY & HEALTH CONSIDERATIONS

The procedures will be implemented in a way consistent with the environment, safety, and health policies of the relevant work areas. Within BNL the process is described in the SBMS: "Work Planning & Control for Experiments and Operations".

The PCBs can be powered up on a table-top for testing for all required testing. This requires a standard computer ATX power supply, which has +12V, +5V, and +3.3V outputs with proper wattage rating. This environment typically does not constitute an ES&H hazard.

5. RECORDS AND DOCUMENTATION

A label reporting a unique numeric identifier shall be placed on each assembled GTU PCBs, and the GTU boxes. The results of all tests shall be labeled according to the numeric identifier.

Table 1. EIC project will provide the following technical documentation (section 6)

File Name	Description	Version
Schematics/GTU_schematics.pdf Schematics/OpticGTU_schematics.pdf	Schematics	1.0
GerberFiles/GTU_gerber.zip GerberFiles/OpticGTU_gerber.zip	Gerber files for bare PCB manufacturing	
BOM/GTU_bom.xlsx BOM/OpticGTU_bom.xlsx	Bill of Materials for PCB assembly	1.0
XYPosition/GTU_XY.txt XYPosition/OpticGTU_XY.txt	Pick & Place for PCB assembly	1.0

5.1. Manufacturer/Producer Records

Printed circuit boards (PCBs) will have manufacturing identifiers (typically stamps on the boards). The QA records for each board will indicate that they passed manufacturing continuity testing. Completed GTU boards will be labeled with a unique ID used to tag all FAT and SAT tests. The source of all commercial off the shelf (COTS) components must be identified. The components shall be assembled and installed to commercial industry standards.

5.2. Deliverable Documentation and Records

The deliverable documentation will consist of:

- A Factory Acceptance Test (FAT) as defined in section 2.1.1 for each GTU (The GTU base board and/or the Optical plug-in Card) module labeled according to its unique identifier.
- The Site Acceptance Test (SAT) as detailed in section 2.1.2 for each GTU (the GTU base board and/or the Optical plug-in card) labeled according to its unique identifier. The output of all BISTs.

6. REFERENCES

Technical Documentation : GTU Manual