

ePIC ZDC-HCal SiPM-on-Tile Boards Inspection and Test Plan

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Abstract

The Zero Degree Calorimeter (ZDC) will be used to identify neutral and charged hadrons at very high pseudorapidity in the ePIC detector. The Silicon Photomultiplier (SiPM)-on-tile design will be tested using cosmic rays and standard electronics continuity and stability tests, to ensure the desired precision for physics measurements is met.

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1. PRODUCT PROPERTIES

The following properties are used to evaluate the functioning of the completed ZDC and its component layers and electronics.

- **PCB Continuity:** Each PCB must have its continuity checked to avoid manufacturer defects or short circuits.
- **Cable Continuity:** The stability of the electronic connection in each cable must be checked manually.
- **Breakdown Voltage:** The PCBs each need to be checked to identify the breakdown voltage using a Keithley Sourcemeter and Python analysis scripts.
- **Pedestal & MIP Peak Identification:** The pedestal value and MIP peak presence or absence need to be verified using cosmic ray measurements for each SiPM channel in the detector.
- **Channel Mapping & DAQ Coordination:** It is necessary to verify that the detector channel mapping is correct and to check the DAQ readout, which is performed using a custom script which synchronizes and allows visualization of cosmic ray tracks within the detector. Self-triggering of the detector is performed via software used to control the CALOROC DAQ system.

2. PROCESSES AND PROCEDURES

2.1. PCB Continuity

2.1.1. In-Process Testing

To ensure there are no manufacturing defects in the PCB layers, each PCB should have their continuity checked with a multimeter. This process involves touching one SiPM pad and its corresponding connector pad to verify connection, and each connector pad with its nearest neighbors to check for shorts.

2.1.2. Failures and Non-Conformances

Any boards that display continuity faults will be discarded and spare boards used instead. Minor or easily accessible faults can be fixed with on-board soldering. If a large number of boards display major manufacturing defects replacements will be ordered.

2.2. Cable Continuity

2.2.1. In-Process Testing

Once each cable is fully constructed, continuity should be checked with a multimeter. This process involves touching each side of the cable for each channel to verify continuity, and checking neighboring pins to check for shorts.

2.2.2. Failures and Non-Conformances

Like the PCBs, cables that display shorts or other faults will be replaced by cables that successfully pass the testing. The planned spare amount of cables is expected to be sufficient to cover any issues that may arise.

2.3. Breakdown Voltage

2.3.1. In-Process Testing

Once a PCB has been fully soldered with SiPMs and connectors, but before tiles are affixed, each channel should be checked with an I-V curve. Place the board inside a dark box, and connect the cable for the test channel to a Keithley 2450 SourceMeter, and run an IV curve test using a LabView program controlling the SourceMeter. Record the output files for each channel, and analyze them using a python script that will detect the breakdown voltage for each channel. If a channel yields a breakdown voltage significantly far from average, if one could not be detected, or otherwise has an abnormal feature in the IV curve, the channel should be re-tested. An abnormal IV curve may simply be the result of the dark box not being sufficiently light tight.

2.3.2. Failures and Non-Conformances

If a channel fails the IV curve a second time, it should be considered faulty. To resolve this, first check the connector pads with a multimeter to ensure there is no short. If it is the result of a faulty SiPM, desolder the SiPM by applying heat to the PCB just underneath the SiPM using a hot air gun and remove the SiPM with plastic tweezers. Then, check the SiPM pads on the PCB with a multimeter to ensure that desoldering did not introduce a short. Finally, solder a new SiPM to this location using the usual method.

2.4. Pedestal & MIP Peak Identification

The completed ZDC modules will record cosmic ray data for the purpose of MIP (Minimum Ionizing Particle) calibration. Events will be collected using the same settings as are planned for full detector operation, but with the trigger logic set to an internal 2 channel trigger.

2.4.1. In-Process Testing

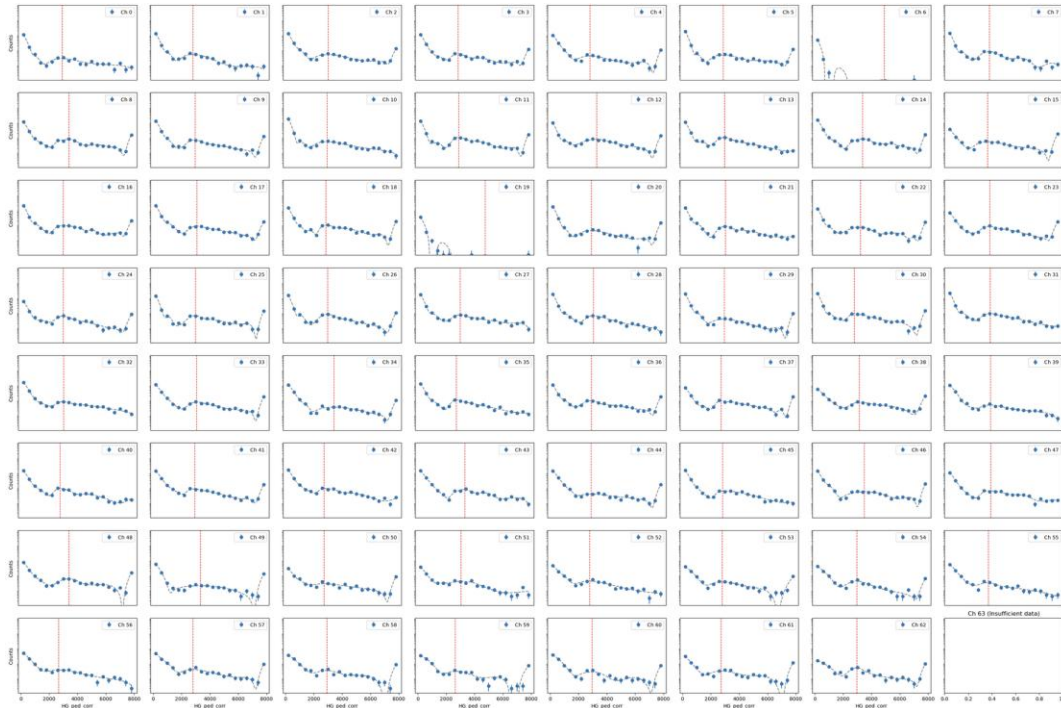


Figure 1. MIP Readout Data from ZDC Engineering Test

Once two PCBs have been fully soldered with SiPMs and connectors, but before tiles are affixed, they should be checked with a cosmic ray test. Cosmic ray data will be collected using the full ZDC readout electronics stack. The HG energy spectra for each channel is then fit to a cubic spline, and the most probable value above the pedestal region are recorded as the MIP energy value for that channel. This test will also be used to measure the mean pedestal for each channel, which will be subtracted out as a baseline to calibrate the detector. First, place (but do not affix) wrapped scintillating tiles on each SiPM for both boards. Next, place one board on top of the other within a dark box using an 8020 frame, as shown below.

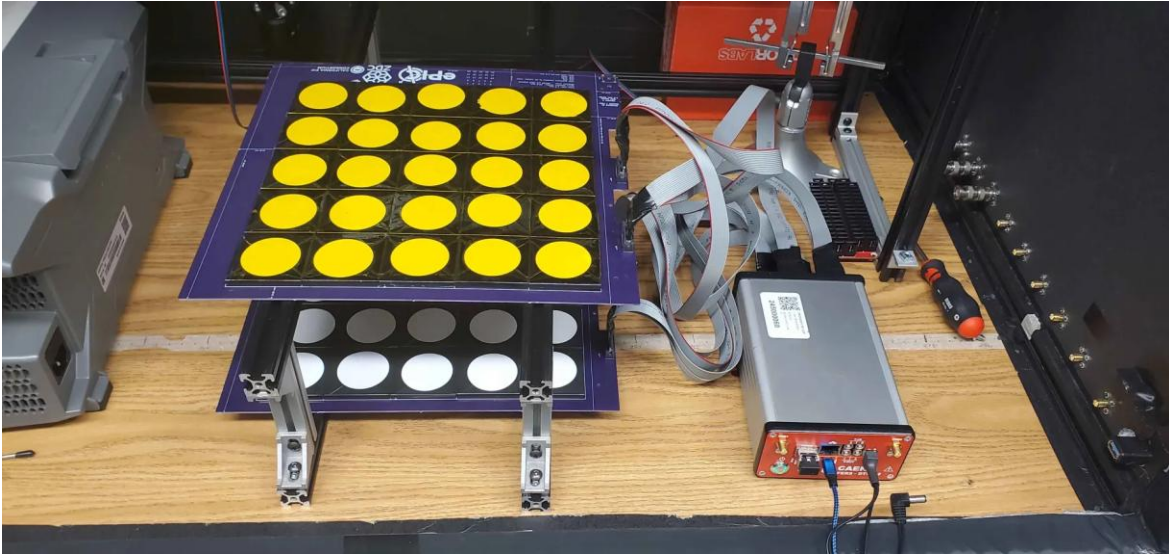


Figure 2. SiPM on tile cosmic ray testing setup

First, with the channels biased, perform a short 10 second periodic trigger run and record the mean pedestal value for each channel. If a channel shows a pedestal significantly far from the mean, or the DAQ system results in an over-voltage error, then re-test the boards with the IV test.

Following the periodic trigger run, run a 10-minute 2-channel trigger run to observe MIP signals from cosmic rays. If a channel is not recording a significant number of above-threshold events in this time period, it should be considered faulty and be I-V tested.

Following a successful 10-minute cosmic ray test, multiple boards can be stacked together for an overnight cosmic ray test for MIP peak identification. Test as many boards simultaneously as the available DAQ system will allow. Plot the resulting pedestal-subtracted high gain distribution for each channel, and analyze it using a MIP-finding python script. The plots should resemble those shown in Figure 1.

2.4.2. Failures and Non-Conformances

Any channel that results in a MIP value that is significantly different from the mean, can't be identified, or otherwise appears anomalous should be retested with the IV test. In the above example, channel 6 and 19 are faulty. The connections and SiPM for this channel will be physically checked and replaced as needed. The MIP calibration will be repeated until functionality can be verified in all channels.

2.5. Channel Mapping & DAQ Coordination

2.5.1. In-Process Testing

Self-triggering of the detector is performed via the DAQ software associated with the CALOROC readout electronics. To confirm event building is functioning as expected, the ZDC modules will be set to record cosmic ray events using a majority-2 internal trigger. A typical event visualization from a cosmic ray event is shown in Figure 3.

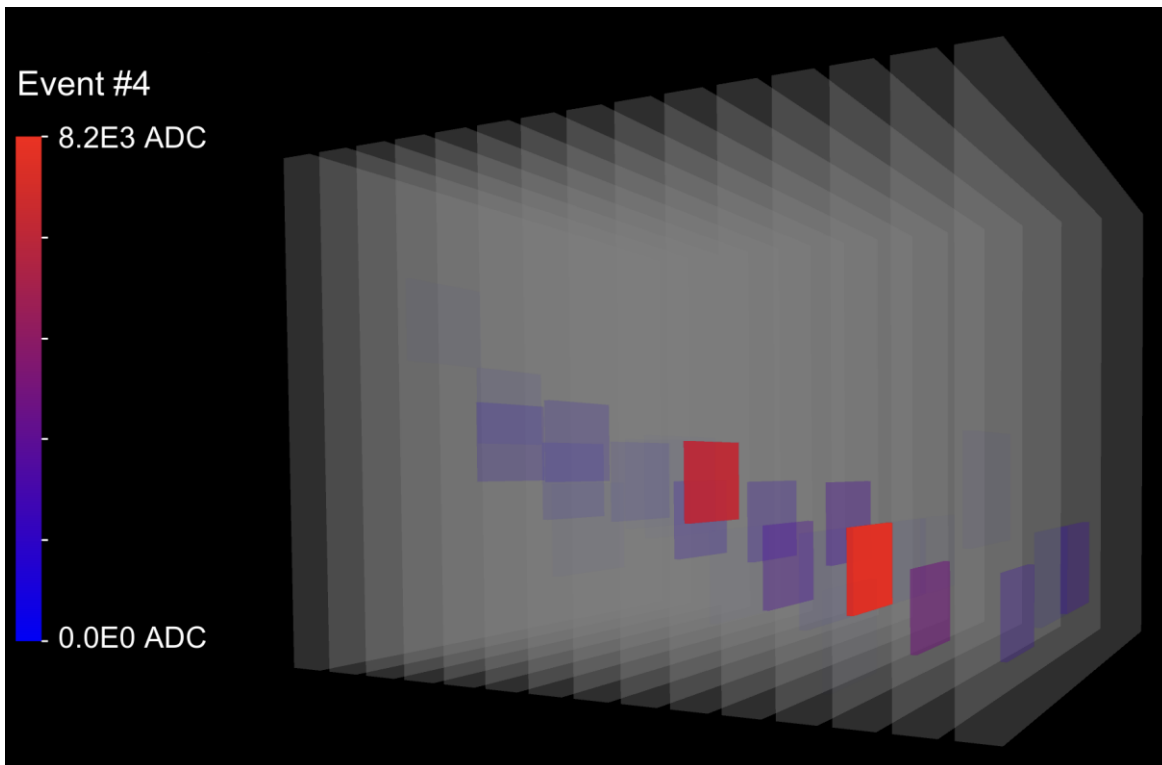


Figure 3. Event Builder visualization of a cosmic ray event

2.5.2. Failures and Non-Conformances

If event building fails the analysis software and custom codes must be subject to troubleshooting, and any layers which do not properly register as part of cosmic ray tracks must be repaired or replaced.

3. EXPERIMENTAL/TEST SETUPS

3.1. Cosmic Ray MIP Testing

The MIP testing requires an appropriate cosmic ray tile testing station, including a CAEN DT5202 unit for readout. In the final verification testing, the CAEN unit will be replaced by CALOROC electronics. A stack of two PCB layers is used inside a large light-tight box.

3.1.1. Resource Requirements

- Wall outlet access

3.1.2. Test Conditions

The test requires a light-tight box large enough to mount two PCB layers on top of each other with an 8020 frame.

3.1.3. Equipment

- CALOROC Readout Board
- Computer running DAQ software

3.2. Breakdown Voltage Evaluation

Measuring the breakdown voltage requires only a light-tight box big enough to fit a PCB, and a Keithley SourceMeter controlled by NI LabView software, which is used to measure the IV curve of the channels.

3.2.1. Resource Requirements

- Wall outlet access

3.2.2. Test Conditions

The test requires a light-tight box large enough to place a PCB layer inside.

3.2.3. Equipment

- Keithley 2450 SourceMeter
- Computer running LabView

4. ENVIRONMENT, SAFETY & HEALTH CONSIDERATIONS

The procedures will be implemented in a way consistent with the environment, safety, and health policies of the relevant work areas. Within Jefferson Lab the process is described in the ES&H manual Chapter 3200, Work Planning and Control Program and at BNL within the SBMS: “Work Planning & Control for Experiments and Operations”. SiPM-on-Tile PCB boards should be handled using clean powder free nitrile gloves at all times.

5. RECORDS AND DOCUMENTATION

5.1. Manufacturer/Producer Records

For every item that is manufactured, the manufacturer will be responsible for maintaining records (travelers) of all raw material that are used in the fabrication process, and document the processes and procedures that were used for production. The resultant documentation will be compiled into a report and will be provided to the project as part of the deliverable, which will be reviewed, validated, and then placed in the central data repository. Manufacturer records will be collected for the final PCBs.

5.2. Deliverable Documentation and Records

We will compile a spreadsheet of initial breakdown voltages, pedestal values, and MIP values for each channel. All testing and inspection data will be provided to the project as part of the final instrument report. Calibrations from the MIP testing will be made available as part of the experimental database as an initial calibration of the detector. Further relative calibrations may be performed with the help of an LED monitoring system.

6. REFERENCES

- [1] EIC Systems Engineering Group, "Requirements Management Plan," Brookhaven National Laboratory, Brookhaven, NY, 2022.
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- [4] M. Arratia and S. Preins, ZDC Engineering Test Module Report, Riverside, CA: University of California Riverside (UCR), 2024.